Specifications Ver. 0.99

Driver LSI for a color TFT LCD Panel

MC2PA8201

Checked by : Keiji Hayashi

Prepared by : Jun Takasu

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This document is subject to change without notice.

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1.Product overview

The MC2PA8201 is a one-chip driver LSI for TFT liquid crystal display with built-in Gate driver I/F.

The MC2PA8201 incorporates 240 TFT Data line drive outputs, built-in Gate driver I/F signals generate circuit, and incorporates 1,843,200bit (240 x 24 x 320) display RAM and can display 1677K Colors.

2.Features

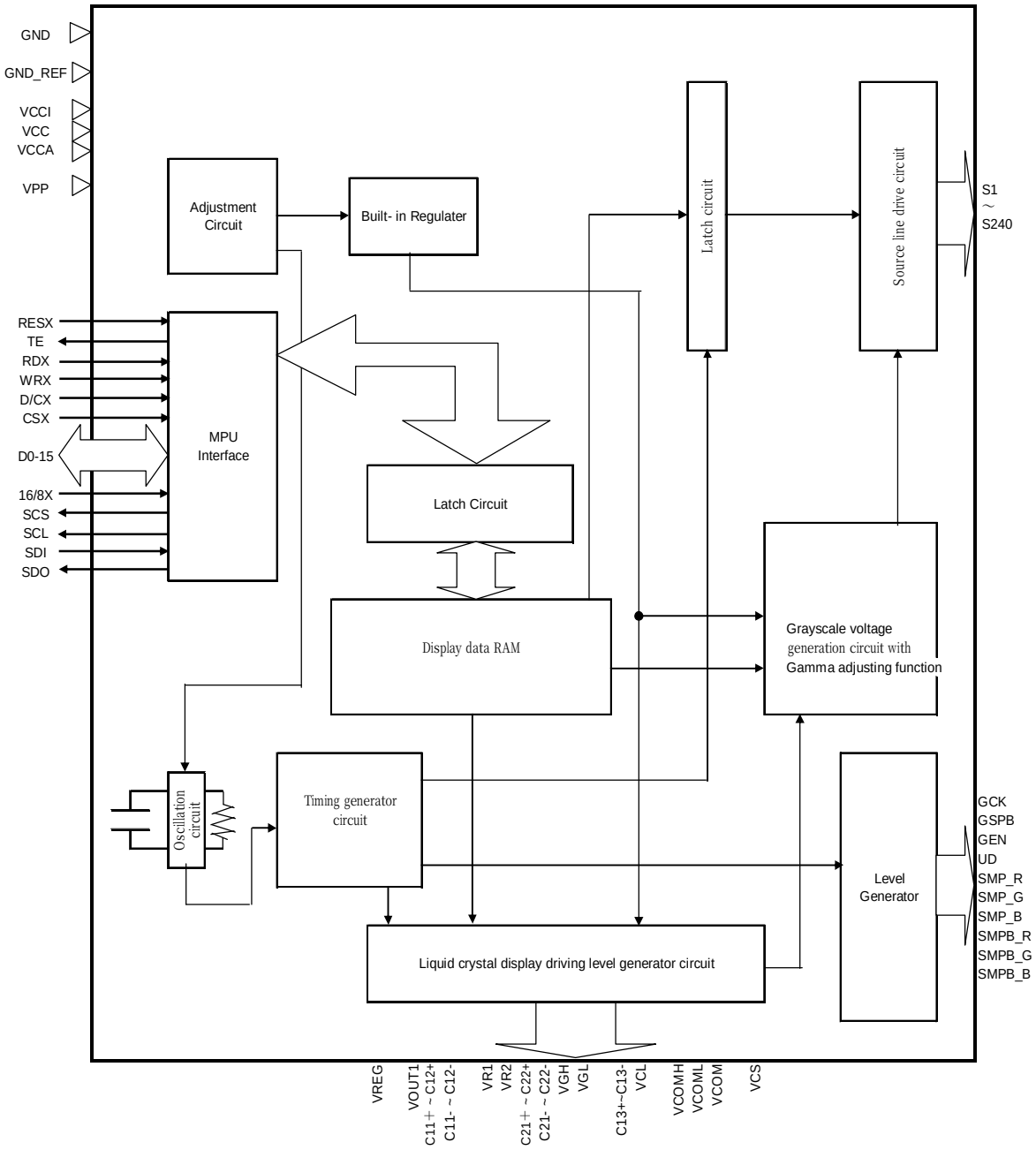
- The MC2PA8201 is a one-chip driver LSI for TFT liquid crystal display with built-in Gate driver I/F.
- Incorporates 8/16bit Parallel I/F, Serial I/F for external EEPROM.
- I/O Circuit power supply（VCCI）: 1.65~1.95V, Power supply（VCC,VCCA）: 2.60~2.95V
- Incorporates display RAM: 240x24x320bits.
- LCD drive I/F

  Source output(S1~S240) : V0~V255 Gray Scale.

  Gate output (VGH,VGL) : CGS-Panel control output are 10 outputs.

  Incorporate VCOM generate circuit.
- Max 1677K Colors
- Incorporate OSC circuit.

3. Block Diagram



4. Pin Assignment

4.1. Pin Description

4.1.1. Power supply pins - 1

Bump No.	Signal	No of pins	I/O	Connected to	Function	Unused pins
101-108, 309-318	VCC	18	I	Power supply and bypass capacitor	Power supply for step-up circuit, power circuit to drive LCD panel and EEPROM interface circuit such as SCS, SCL and SDO. Connect to external 2.60V to 2.95V power supply.	-
117	VPP	1	I	Power supply	Power supply for inside EEPROM. Connect to VCC pin.	VCC
183-198	VCCA	16	I	Power supply and bypass capacitor	Power supply for analog reference voltage generator. Connect to VCC on FPC not on Glass.	-
241-248	VCCI	8	I	Power supply and bypass capacitor	Power supply for interface circuit such as CSX, RDX, WRX, D15-0, D/CX, RESEX, 16/8x, TE) and for built-in RAM and logic circuit. Connect to external 1.65V to 1.95V power supply.	-
172-182	GND_REF	11	-	GND	GND for analog reference voltage generator. Connect to GND on FPC, not on TFT panel.	-
142-154, 161, 233-240, 307-308, 323-325	GND	27	-	GND	GND pins. Connect to 0V.	-

4.1.2. Power supply pins - 2

Bump No.	Signal	No of pins	I/O	Connected to	Function	Unused pins	未使用時処理
92-100	VOUT1	9	O	Bypass capacitor	Step-upped voltage from step-up circuit 1.	VCC	-
109-115	VR1	7	O	Bypass capacitor	Regulator output for step-up circuit 2.	GND	-
199-208	VR2	10	O	Bypass capacitor	Regulator output for step-up circuit 2.	GND	-
45-51,	VGH	7	O	Bypass capacitor	TFT LCD drive power supply from step-up circuit 2.	GND	-
329	VGHO	1	O	TFT LCD panel	TFT LCD drive power supply from step-up circuit 2. By switch control, it output a VGH level by the same timing to VGL.	GND	-
54-63, 330	VGL	10+1	O	Bypass capacitor TFT LCD panel	TFT LCD drive power supply from step-up circuit 2. It output the Gate off level.	GND	-
65-69	VCL	5	O	Bypass capacitor	Power supply for VCOML circuit from step-up circuit 3. It become power supply to VCOML circuit.	GND	-

4.1.3. Step up Capacitor pins

Bump No.	Signal	No. of Pins	I/O	Connected to	Function	After reset	Unused pins
71-75	C11+	5	I/O	C11- through step-up capacitor	Step-up capacitor connection for step-up 1.	VCC	-
76-80	C11-	5	I/O	C11+ through step-up capacitor	Step-up capacitor connection for step-up 1.	GND	-
81-85	C12+	5	I/O	C12- through step-up capacitor	Step-up capacitor connection for step-up 1.	VCC	
86-90	C12-	5	I/O	C12+ through step-up capacitor	Step-up capacitor connection for step-up 1.	GND	
37-39	C13+	3	I/O	C13- through step-up capacitor	Step-up capacitor connection for step-up 3.	GND	
41-43	C13-	3	I/O	C13+ through step-up capacitor	Step-up capacitor connection for step-up 3.	GND	
30-32	C21+	3	I/O	C21- through step-up capacitor	Step-up capacitor connection for step-up 2.	GND	
33-35	C21-	3	I/O	C21+ through step-up capacitor	Step-up capacitor connection for step-up 2.	GND	
24-26	C22+	3	I/O	C22- through Step-up capacitor	Step-up capacitor connection for step-up 2.	GND	
27-29	C22-	3	I/O	C22+ through step-up capacitor	Step-up capacitor connection for step-up 2.	GND	

4.1.4. Interface pins

Bump No.	Signal	No. of Pins	I/O	Connected to	Function	After reset	Unused pins
257	CSX	1	I	MPU	Chip select signal. (Amplitude: VCCI – GND) “Low”: Selection (Possible to access trough parallel interface) “High” Non-selection (Impossible to access through parallel interface)	-	-
256	D/CX	1	I	MPU	Command/Data select signal. (Amplitude: VCCI – GND) “Low”: Command “High” Data	-	-
281	RESX	1	I	MPU or external CR circuit	Reset signal. (Amplitude: VCCI – GND) Initialization at “Low”. Power on reset shall be done after power supply.	-	-
255	WRX	1	I	MPU	Write strobe signal. (Amplitude: VCCI – GND) Data is written at rising edge.	-	-
254	RDX	1	I	MPU	Read strobe signal. (Amplitude: VCCI – GND) Data is read at “Low” level .	-	-
258-263, 267-276	D0 D5 D6-D15	16	I/O	MPU	16-bit bidirectional data bath. (Amplitude: VCCI – GND) 8-bit interface: D7 to D0 are used. (D15 to D8 are connected to GND or VCCI) 16-bit interface: D15 to D0 are used.	-	GND or VCCI
277	16/8X	1	I	MPU	Data bath width selection. (Amplitude: VCCI – GND) “Low”: 8-bit interface “High”: 16-bit interface	-	-
253	TE	1	O	MPU	Tearing effect output signal. (Amplitude: VCCI – GND)	GND	-
225	SCS	1	O	EEPROM	EEPROM select signal. (Amplitude: VCC – GND) “Low”: Non-selection (Impossible to access) “High”: Selection (Possible to access)	GND	Open
226	SCL	1	O	EEPROM	Serial clock signal. (Amplitude: VCC– GND)	GND	Open
227	SDI	1	I	EEPROM	EEPROM data input signal. (Amplitude: VCC – GND) Serial data input.	-	-
228	SDO	1	O	EEPROM	EEPROM data output signal. (Amplitude: VCC– GND) Start-bit, Operand, Address and serial data output.	GND	Open

4.1.5. TFT LCD drive pins

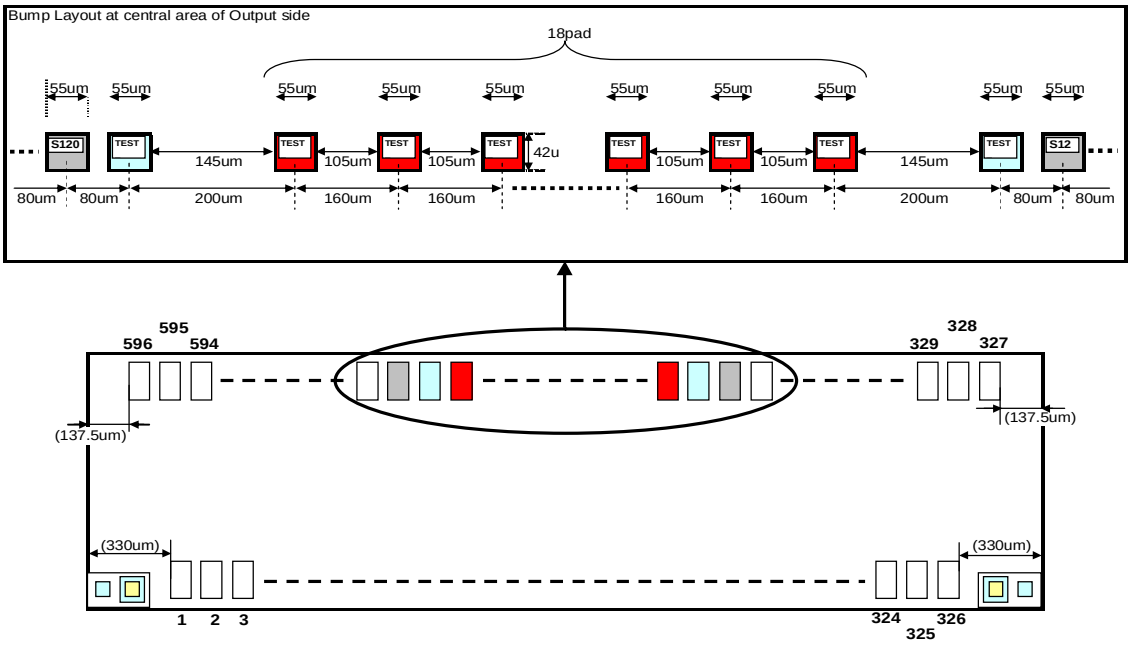
Bump No.	Signal	No. of Pins	I/O	Connected to	Function	After Reset	Unused pins
155-157	VREG	3	O	Bypass capacitor	Built-in regulator output Used for the reference voltage of source driver gray scale, VCOM center and VCOM amplitude.	GND	-
125-129	VCOM	5	O	TFT LCD panel	TFT LCD panel common node drive output. Alternative output between VCOMH and VCOML.	GND	-
136-141	VCOMH	6	O	Bypass capacitor	VCOM high level output.	GND	-
130-135	VCOML	6	O	Bypass capacitor	VCOM low level output pin.	GND	-
591-472, 451-332	S1-S120, S121-S240	240	O	TFT LCD panel	Source line output for LCD panel	GND	-
5-6	GCK	2	O	TFT LCD panel	Gate clock signal (Amplitude: VGH – VGL)	GND	-
3-4	GSPB	2	O	TFT LCD panel	Gate start pulse signal (Amplitude: VGH – VGL)	GND	-
9-10	GEN	2	O	TFT LCD panel	Gate enable signal (Amplitude: VGH – VGL)	GND	-
7-8	UD	2	O	TFT LCD panel	Up/Down signal (Amplitude: VGH – VGL)	GND	-
17-18	SMP_R	2	O	TFT LCD panel	<R> Selection signal pin (Amplitude: VGH – VGL)	GND	-
19-20	SMP_G	2	O	TFT LCD panel	<G> Selection signal pin (Amplitude: VGH – VGL)	GND	-
21-22	SMP_B	2	O	TFT LCD panel	<B> Selection signal pin (Amplitude: VGH – VGL)	GND	-
11-12	SMPB_R	2	O	TFT LCD panel	<R> Selection signal pin VGH – VGL amplitude and inverted signal of SMP_R	GND	-
13-14	SMPB_G	2	O	TFT LCD panel	<G> Selection signal pin VGH – VGL amplitude and inverted signal of SMP_G	GND	-
15-16	SMPB_B	2	O	TFT LCD panel	<B> Selection signal pin VGH – VGL amplitude and inverted signal of SMP_B	GND	-
121-124	VCS	4	O	TFT LCD common node /Bypass capacitor	Sub capacitor drive. Minimum drive voltage output	GND	-

4.1.6. TEST pins

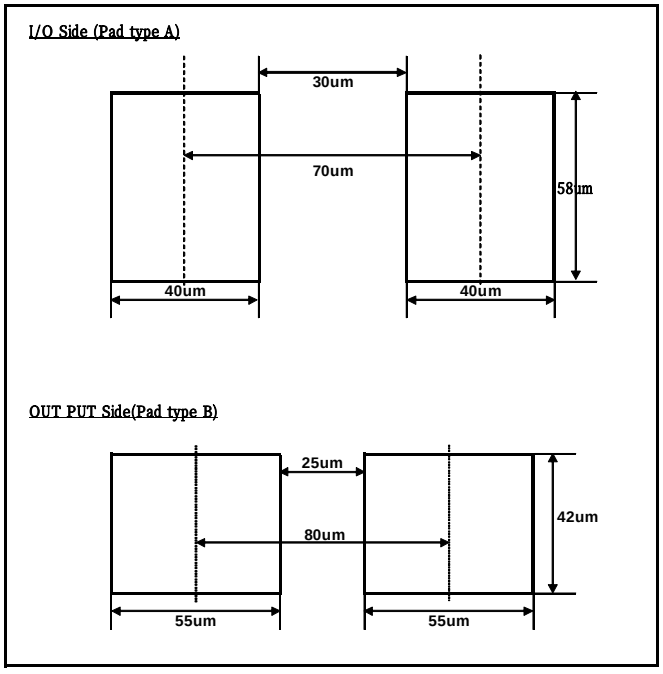
Bump No.	Signal	No. of Pins	I/O	Connected to	Function	Unused pins
1,91,116, 118-120, 158-160, 162-171, 209-215, 217, 219-224, 229-232, 249-252, 264-266, 278-280, 282-294, 303-306, 326 453-470, 593-596	TEST_OPEN	87	-	Open	Test pin Leave it open. They have no ESD elements.	Open
327,328	TEST_ESD	2	-	Open	Test pin with ESD protect circuits whose high voltage is VGH and Low voltage is VGL.	Open
216, 218, 295-302, 319-322	TEST_GND	14	-	GND	Test pin Connect to GND on panel	GND
2, 23, 36, 40, 44, 52, 53, 64, 70, , 331, 452, 471, 592	TEST_OG	13	-	GND or Open	Test pin Connect to GND on panel or leave it open	GND or Open

4.2. Bump Layout

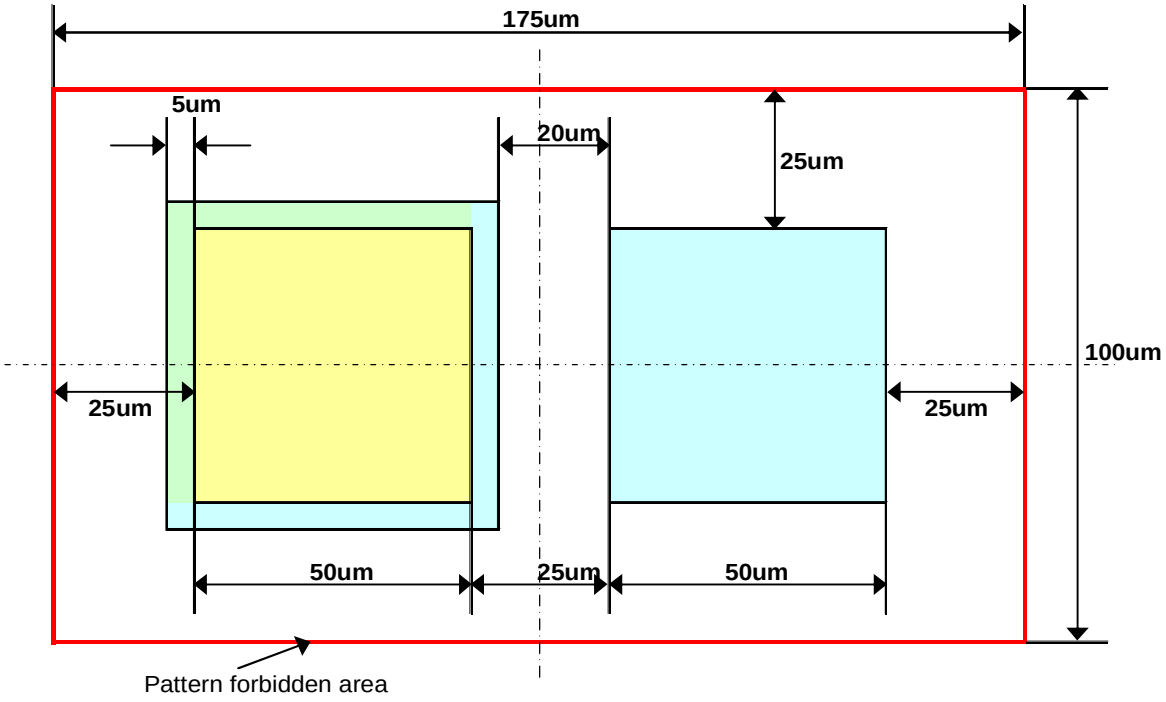
4.2.1. Bump Placement

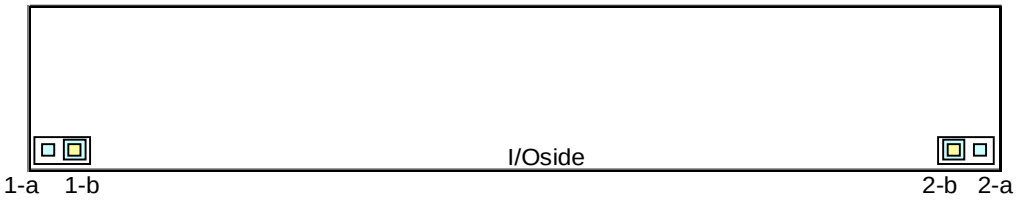


4.2.2. Bump Size



4.2.3. Alignment Mark





Alignment Coordinate:

	X(μm)	Y(μm)
1-a: Metal	-11597.0	-662.0
1-b: Bump	-11522.0	-662.0
2-a: Metal	11597.0	-662.0
2-b: Bump	11522.0	-662.0

5. Bump Coordinate

Pad No	Pad Name	X	Y
1	TEST_OPEN	-11375	-691.5
2	TEST_OG	-11305	-691.5
3	GSPB	-11235	-691.5
4	GSPB	-11165	-691.5
5	GCK	-11095	-691.5
6	GCK	-11025	-691.5
7	UD	-10955	-691.5
8	UD	-10885	-691.5
9	GEN	-10815	-691.5
10	GEN	-10745	-691.5
11	SMPB_R	-10675	-691.5
12	SMPB_R	-10605	-691.5
13	SMPB_G	-10535	-691.5
14	SMPB_G	-10465	-691.5
15	SMPB_B	-10395	-691.5
16	SMPB_B	-10325	-691.5
17	SMP_R	-10255	-691.5
18	SMP_R	-10185	-691.5
19	SMP_G	-10115	-691.5
20	SMP_G	-10045	-691.5
21	SMP_B	-9975	-691.5
22	SMP_B	-9905	-691.5
23	TEST_OG	-9835	-691.5
24	C22P	-9765	-691.5
25	C22P	-9695	-691.5
26	C22P	-9625	-691.5
27	C22M	-9555	-691.5
28	C22M	-9485	-691.5
29	C22M	-9415	-691.5
30	C21P	-9345	-691.5
31	C21P	-9275	-691.5
32	C21P	-9205	-691.5
33	C21M	-9135	-691.5
34	C21M	-9065	-691.5
35	C21M	-8995	-691.5
36	TEST_OG	-8925	-691.5
37	C13P	-8855	-691.5
38	C13P	-8785	-691.5
39	C13P	-8715	-691.5
40	TEST_OG	-8645	-691.5
41	C13M	-8575	-691.5
42	C13M	-8505	-691.5
43	C13M	-8435	-691.5
44	TEST_OG	-8365	-691.5
45	VGH	-8295	-691.5
46	VGH	-8225	-691.5
47	VGH	-8155	-691.5
48	VGH	-8085	-691.5
49	VGH	-8015	-691.5
50	VGH	-7945	-691.5

Pad No	Pad Name	X	Y
51	VGH	-7875	-691.5
52	TEST_OG	-7805	-691.5
53	TEST_OG	-7735	-691.5
54	VGL	-7665	-691.5
55	VGL	-7595	-691.5
56	VGL	-7525	-691.5
57	VGL	-7455	-691.5
58	VGL	-7385	-691.5
59	VGL	-7315	-691.5
60	VGL	-7245	-691.5
61	VGL	-7175	-691.5
62	VGL	-7105	-691.5
63	VGL	-7035	-691.5
64	TEST_OG	-6965	-691.5
65	VCL	-6895	-691.5
66	VCL	-6825	-691.5
67	VCL	-6755	-691.5
68	VCL	-6685	-691.5
69	VCL	-6615	-691.5
70	TEST_OG	-6545	-691.5
71	C11P	-6475	-691.5
72	C11P	-6405	-691.5
73	C11P	-6335	-691.5
74	C11P	-6265	-691.5
75	C11P	-6195	-691.5
76	C11M	-6125	-691.5
77	C11M	-6055	-691.5
78	C11M	-5985	-691.5
79	C11M	-5915	-691.5
80	C11M	-5845	-691.5
81	C12P	-5775	-691.5
82	C12P	-5705	-691.5
83	C12P	-5635	-691.5
84	C12P	-5565	-691.5
85	C12P	-5495	-691.5
86	C12M	-5425	-691.5
87	C12M	-5355	-691.5
88	C12M	-5285	-691.5
89	C12M	-5215	-691.5
90	C12M	-5145	-691.5
91	TEST_OPEN	-5075	-691.5
92	VOUT1	-5005	-691.5
93	VOUT1	-4935	-691.5
94	VOUT1	-4865	-691.5
95	VOUT1	-4795	-691.5
96	VOUT1	-4725	-691.5
97	VOUT1	-4655	-691.5
98	VOUT1	-4585	-691.5
99	VOUT1	-4515	-691.5
100	VOUT1	-4445	-691.5

Pad No	Pad Name	X	Y
101	VCC	-4375	-691.5
102	VCC	-4305	-691.5
103	VCC	-4235	-691.5
104	VCC	-4165	-691.5
105	VCC	-4095	-691.5
106	VCC	-4025	-691.5
107	VCC	-3955	-691.5
108	VCC	-3885	-691.5
109	VR1	-3815	-691.5
110	VR1	-3745	-691.5
111	VR1	-3675	-691.5
112	VR1	-3605	-691.5
113	VR1	-3535	-691.5
114	VR1	-3465	-691.5
115	VR1	-3395	-691.5
116	TEST_OPEN	-3325	-691.5
117	VPP	-3255	-691.5
118	TEST_OPEN	-3185	-691.5
119	TEST_OPEN	-3115	-691.5
120	TEST_OPEN	-3045	-691.5
121	VCS	-2975	-691.5
122	VCS	-2905	-691.5
123	VCS	-2835	-691.5
124	VCS	-2765	-691.5
125	VCOM	-2695	-691.5
126	VCOM	-2625	-691.5
127	VCOM	-2555	-691.5
128	VCOM	-2485	-691.5
129	VCOM	-2415	-691.5
130	VCOML	-2345	-691.5
131	VCOML	-2275	-691.5
132	VCOML	-2205	-691.5
133	VCOML	-2135	-691.5
134	VCOML	-2065	-691.5
135	VCOML	-1995	-691.5
136	VCOMH	-1925	-691.5
137	VCOMH	-1855	-691.5
138	VCOMH	-1785	-691.5
139	VCOMH	-1715	-691.5
140	VCOMH	-1645	-691.5
141	VCOMH	-1575	-691.5
142	GND	-1505	-691.5
143	GND	-1435	-691.5
144	GND	-1365	-691.5
145	GND	-1295	-691.5
146	GND	-1225	-691.5
147	GND	-1155	-691.5
148	GND	-1085	-691.5
149	GND	-1015	-691.5
150	GND	-945	-691.5

Pad No	Pad Name	X	Y
151	GND	-875	-691.5
152	GND	-805	-691.5
153	GND	-735	-691.5
154	GND	-665	-691.5
155	VREG	-595	-691.5
156	VREG	-525	-691.5
157	VREG	-455	-691.5
158	TEST_OPEN	-385	-691.5
159	TEST_OPEN	-315	-691.5
160	TEST_OPEN	-245	-691.5
161	GND	-175	-691.5
162	TEST_OPEN	-105	-691.5
163	TEST_OPEN	-35	-691.5
164	TEST_OPEN	35	-691.5
165	TEST_OPEN	105	-691.5
166	TEST_OPEN	175	-691.5
167	TEST_OPEN	245	-691.5
168	TEST_OPEN	315	-691.5
169	TEST_OPEN	385	-691.5
170	TEST_OPEN	455	-691.5
171	TEST_OPEN	525	-691.5
172	GND_REF	595	-691.5
173	GND_REF	665	-691.5
174	GND_REF	735	-691.5
175	GND_REF	805	-691.5
176	GND_REF	875	-691.5
177	GND_REF	945	-691.5
178	GND_REF	1015	-691.5
179	GND_REF	1085	-691.5
180	GND_REF	1155	-691.5
181	GND_REF	1225	-691.5
182	GND_REF	1295	-691.5
183	VCCA	1365	-691.5
184	VCCA	1435	-691.5
185	VCCA	1505	-691.5
186	VCCA	1575	-691.5
187	VCCA	1645	-691.5
188	VCCA	1715	-691.5
189	VCCA	1785	-691.5
190	VCCA	1855	-691.5
191	VCCA	1925	-691.5
192	VCCA	1995	-691.5
193	VCCA	2065	-691.5
194	VCCA	2135	-691.5
195	VCCA	2205	-691.5
196	VCCA	2275	-691.5
197	VCCA	2345	-691.5
198	VCCA	2415	-691.5
199	VR2	2485	-691.5
200	VR2	2555	-691.5

Pad No	Pad Name	X	Y
201	VR2	2625	-691.5
202	VR2	2695	-691.5
203	VR2	2765	-691.5
204	VR2	2835	-691.5
205	VR2	2905	-691.5
206	VR2	2975	-691.5
207	VR2	3045	-691.5
208	VR2	3115	-691.5
209	TEST_OPEN	3185	-691.5
210	TEST_OPEN	3255	-691.5
211	TEST_OPEN	3325	-691.5
212	TEST_OPEN	3395	-691.5
213	TEST_OPEN	3465	-691.5
214	TEST_OPEN	3535	-691.5
215	TEST_OPEN	3605	-691.5
216	TEST_GND	3675	-691.5
217	TEST_OPEN	3745	-691.5
218	TEST_GND	3815	-691.5
219	TEST_OPEN	3885	-691.5
220	TEST_OPEN	3955	-691.5
221	TEST_OPEN	4025	-691.5
222	TEST_OPEN	4095	-691.5
223	TEST_OPEN	4165	-691.5
224	TEST_OPEN	4235	-691.5
225	SCS	4305	-691.5
226	SCL	4375	-691.5
227	SDI	4445	-691.5
228	SDO	4515	-691.5
229	TEST_OPEN	4585	-691.5
230	TEST_OPEN	4655	-691.5
231	TEST_OPEN	4725	-691.5
232	TEST_OPEN	4795	-691.5
233	GND	4865	-691.5
234	GND	4935	-691.5
235	GND	5005	-691.5
236	GND	5075	-691.5
237	GND	5145	-691.5
238	GND	5215	-691.5
239	GND	5285	-691.5
240	GND	5355	-691.5
241	VCCI	5425	-691.5
242	VCCI	5495	-691.5
243	VCCI	5565	-691.5
244	VCCI	5635	-691.5
245	VCCI	5705	-691.5
246	VCCI	5775	-691.5
247	VCCI	5845	-691.5
248	VCCI	5915	-691.5
249	TEST_OPEN	5985	-691.5
250	TEST_OPEN	6055	-691.5

Pad No	Pad Name	X	Y
251	TEST_OPEN	6125	-691.5
252	TEST_OPEN	6195	-691.5
253	TE	6265	-691.5
254	RDX	6335	-691.5
255	WRX	6405	-691.5
256	D/CX	6475	-691.5
257	CSX	6545	-691.5
258	D0	6615	-691.5
259	D1	6685	-691.5
260	D2	6755	-691.5
261	D3	6825	-691.5
262	D4	6895	-691.5
263	D5	6965	-691.5
264	TEST_OPEN	7035	-691.5
265	TEST_OPEN	7105	-691.5
266	TEST_OPEN	7175	-691.5
267	D6	7245	-691.5
268	D7	7315	-691.5
269	D8	7385	-691.5
270	D9	7455	-691.5
271	D10	7525	-691.5
272	D11	7595	-691.5
273	D12	7665	-691.5
274	D13	7735	-691.5
275	D14	7805	-691.5
276	D15	7875	-691.5
277	16/8X	7945	-691.5
278	TEST_OPEN	8015	-691.5
279	TEST_OPEN	8085	-691.5
280	TEST_OPEN	8155	-691.5
281	RESX	8225	-691.5
282	TEST_OPEN	8295	-691.5
283	TEST_OPEN	8365	-691.5
284	TEST_OPEN	8435	-691.5
285	TEST_OPEN	8505	-691.5
286	TEST_OPEN	8575	-691.5
287	TEST_OPEN	8645	-691.5
288	TEST_OPEN	8715	-691.5
289	TEST_OPEN	8785	-691.5
290	TEST_OPEN	8855	-691.5
291	TEST_OPEN	8925	-691.5
292	TEST_OPEN	8995	-691.5
293	TEST_OPEN	9065	-691.5
294	TEST_OPEN	9135	-691.5
295	TEST_GND	9205	-691.5
296	TEST_GND	9275	-691.5
297	TEST_GND	9345	-691.5
298	TEST_GND	9415	-691.5
299	TEST_GND	9485	-691.5
300	TEST_GND	9555	-691.5

Pad No	Pad Name	X	Y
301	TEST_GND	9625	-691.5
302	TEST_GND	9695	-691.5
303	TEST_OPEN	9765	-691.5
304	TEST_OPEN	9835	-691.5
305	TEST_OPEN	9905	-691.5
306	TEST_OPEN	9975	-691.5
307	GND	10045	-691.5
308	GND	10115	-691.5
309	VCC	10185	-691.5
310	VCC	10255	-691.5
311	VCC	10325	-691.5
312	VCC	10395	-691.5
313	VCC	10465	-691.5
314	VCC	10535	-691.5
315	VCC	10605	-691.5
316	VCC	10675	-691.5
317	VCC	10745	-691.5
318	VCC	10815	-691.5
319	TEST_GND	10885	-691.5
320	TEST_GND	10955	-691.5
321	TEST_GND	11025	-691.5
322	TEST_GND	11095	-691.5
323	GND	11165	-691.5
324	GND	11235	-691.5
325	GND	11305	-691.5
326	TEST_OPEN	11375	-691.5
327	TEST_ESD	11560	706
328	TEST_ESD	11480	706
329	VGH	11400	706
330	VGL	11320	706
331	TEST_OG	11240	706
332	S240	11160	706
333	S239	11080	706
334	S238	11000	706
335	S237	10920	706
336	S236	10840	706
337	S235	10760	706
338	S234	10680	706
339	S233	10600	706
340	S232	10520	706
341	S231	10440	706
342	S230	10360	706
343	S229	10280	706
344	S228	10200	706
345	S227	10120	706
346	S226	10040	706
347	S225	9960	706
348	S224	9880	706
349	S223	9800	706
350	S222	9720	706

Pad No	Pad Name	X	Y
351	S221	9640	706
352	S220	9560	706
353	S219	9480	706
354	S218	9400	706
355	S217	9320	706
356	S216	9240	706
357	S215	9160	706
358	S214	9080	706
359	S213	9000	706
360	S212	8920	706
361	S211	8840	706
362	S210	8760	706
363	S209	8680	706
364	S208	8600	706
365	S207	8520	706
366	S206	8440	706
367	S205	8360	706
368	S204	8280	706
369	S203	8200	706
370	S202	8120	706
371	S201	8040	706
372	S200	7960	706
373	S199	7880	706
374	S198	7800	706
375	S197	7720	706
376	S196	7640	706
377	S195	7560	706
378	S194	7480	706
379	S193	7400	706
380	S192	7320	706
381	S191	7240	706
382	S190	7160	706
383	S189	7080	706
384	S188	7000	706
385	S187	6920	706
386	S186	6840	706
387	S185	6760	706
388	S184	6680	706
389	S183	6600	706
390	S182	6520	706
391	S181	6440	706
392	S180	6360	706
393	S179	6280	706
394	S178	6200	706
395	S177	6120	706
396	S176	6040	706
397	S175	5960	706
398	S174	5880	706
399	S173	5800	706
400	S172	5720	706

Pad No	Pad Name	X	Y
401	S171	5640	706
402	S170	5560	706
403	S169	5480	706
404	S168	5400	706
405	S167	5320	706
406	S166	5240	706
407	S165	5160	706
408	S164	5080	706
409	S163	5000	706
410	S162	4920	706
411	S161	4840	706
412	S160	4760	706
413	S159	4680	706
414	S158	4600	706
415	S157	4520	706
416	S156	4440	706
417	S155	4360	706
418	S154	4280	706
419	S153	4200	706
420	S152	4120	706
421	S151	4040	706
422	S150	3960	706
423	S149	3880	706
424	S148	3800	706
425	S147	3720	706
426	S146	3640	706
427	S145	3560	706
428	S144	3480	706
429	S143	3400	706
430	S142	3320	706
431	S141	3240	706
432	S140	3160	706
433	S139	3080	706
434	S138	3000	706
435	S137	2920	706
436	S136	2840	706
437	S135	2760	706
438	S134	2680	706
439	S133	2600	706
440	S132	2520	706
441	S131	2440	706
442	S130	2360	706
443	S129	2280	706
444	S128	2200	706
445	S127	2120	706
446	S126	2040	706
447	S125	1960	706
448	S124	1880	706
449	S123	1800	706
450	S122	1720	706

Pad No	Pad Name	X	Y
451	S121	1640	706
452	TEST_OG	1560	706
453	TEST_OPEN	1360	706
454	TEST_OPEN	1200	706
455	TEST_OPEN	1040	706
456	TEST_OPEN	880	706
457	TEST_OPEN	720	706
458	TEST_OPEN	560	706
459	TEST_OPEN	400	706
460	TEST_OPEN	240	706
461	TEST_OPEN	80	706
462	TEST_OPEN	-80	706
463	TEST_OPEN	-240	706
464	TEST_OPEN	-400	706
465	TEST_OPEN	-560	706
466	TEST_OPEN	-720	706
467	TEST_OPEN	-880	706
468	TEST_OPEN	-1040	706
469	TEST_OPEN	-1200	706
470	TEST_OPEN	-1360	706
471	TEST_OG	-1560	706
472	S120	-1640	706
473	S119	-1720	706
474	S118	-1800	706
475	S117	-1880	706
476	S116	-1960	706
477	S115	-2040	706
478	S114	-2120	706
479	S113	-2200	706
480	S112	-2280	706
481	S111	-2360	706
482	S110	-2440	706
483	S109	-2520	706
484	S108	-2600	706
485	S107	-2680	706
486	S106	-2760	706
487	S105	-2840	706
488	S104	-2920	706
489	S103	-3000	706
490	S102	-3080	706
491	S101	-3160	706
492	S100	-3240	706
493	S99	-3320	706
494	S98	-3400	706
495	S97	-3480	706
496	S96	-3560	706
497	S95	-3640	706
498	S94	-3720	706
499	S93	-3800	706
500	S92	-3880	706

Pad No	Pad Name	X	Y
501	S91	-3960	706
502	S90	-4040	706
503	S89	-4120	706
504	S88	-4200	706
505	S87	-4280	706
506	S86	-4360	706
507	S85	-4440	706
508	S84	-4520	706
509	S83	-4600	706
510	S82	-4680	706
511	S81	-4760	706
512	S80	-4840	706
513	S79	-4920	706
514	S78	-5000	706
515	S77	-5080	706
516	S76	-5160	706
517	S75	-5240	706
518	S74	-5320	706
519	S73	-5400	706
520	S72	-5480	706
521	S71	-5560	706
522	S70	-5640	706
523	S69	-5720	706
524	S68	-5800	706
525	S67	-5880	706
526	S66	-5960	706
527	S65	-6040	706
528	S64	-6120	706
529	S63	-6200	706
530	S62	-6280	706
531	S61	-6360	706
532	S60	-6440	706
533	S59	-6520	706
534	S58	-6600	706
535	S57	-6680	706
536	S56	-6760	706
537	S55	-6840	706
538	S54	-6920	706
539	S53	-7000	706
540	S52	-7080	706
541	S51	-7160	706
542	S50	-7240	706
543	S49	-7320	706
544	S48	-7400	706
545	S47	-7480	706
546	S46	-7560	706
547	S45	-7640	706
548	S44	-7720	706
549	S43	-7800	706
550	S42	-7880	706

Pad No	Pad Name	X	Y
551	S41	-7960	706
552	S40	-8040	706
553	S39	-8120	706
554	S38	-8200	706
555	S37	-8280	706
556	S36	-8360	706
557	S35	-8440	706
558	S34	-8520	706
559	S33	-8600	706
560	S32	-8680	706
561	S31	-8760	706
562	S30	-8840	706
563	S29	-8920	706
564	S28	-9000	706
565	S27	-9080	706
566	S26	-9160	706
567	S25	-9240	706
568	S24	-9320	706
569	S23	-9400	706
570	S22	-9480	706
571	S21	-9560	706
572	S20	-9640	706
573	S19	-9720	706
574	S18	-9800	706
575	S17	-9880	706
576	S16	-9960	706
577	S15	-10040	706
578	S14	-10120	706
579	S13	-10200	706
580	S12	-10280	706
581	S11	-10360	706
582	S10	-10440	706
583	S9	-10520	706
584	S8	-10600	706
585	S7	-10680	706
586	S6	-10760	706
587	S5	-10840	706
588	S4	-10920	706
589	S3	-11000	706
590	S2	-11080	706
591	S1	-11160	706
592	TEST_OG	-11240	706
593	TEST_OPEN	-11320	706
594	TEST_OPEN	-11400	706
595	TEST_OPEN	-11480	706
596	TEST_OPEN	-11560	706

6. Function Description

6.1. DC/DC Converter

6.1.1. Power supply spec

Table6.1.1-1. External supply voltage

Pin Name	Connect to	Function	Note
VCCI	Bypass capacitor	Power supply for Logic and I/F circuits.	1.65V ~ 1.95V
VCC	Bypass capacitor	Power supply for LCD drive signal generate circuit.	2.60V ~ 2.95V
VCCA	VCC	Power supply for reference voltage	2.60V ~ 2.95V

Table6.1.1-2 Inside generate voltage

Pin Name	Connect to	Function	Note
VOUT1	Bypass capacitor	VOUT1=2xVCC	
VREG	Bypass capacitor	Regulator output for analog circuit	VREG<VOUT1-0.3V
VR1	Bypass capacitor	Regulator output for VGH,VGL	VR1<VOUT1-0.5V
VR2	Bypass capacitor	Regulator output for VGH and VGL	VR2<VOUT1-0.5V
VGH	Bypass capacitor	Power supply for TFT LCD VGH=2xVR1+VR2	9.0V ~ 10.5V
VGL	Bypass capacitor	Power supply for TFT LCD VGL=(-1)x(VR1+VR2)	-6.75V ~ -5.25V
VCL	Bypass capacitor	Power supply for VCOML circuit VCL=(-1)xVCC.	
VCOMH	Bypass capacitor	Power supply for VCOM high level output	2.91V ~ 4.6V at VREG=4.6V
VCOML	Bypass capacitor	Power supply for VCOM low level output	-1.37V ~ 0.48V VCOML>VCL+0.5V

6.1.2. Step up chart

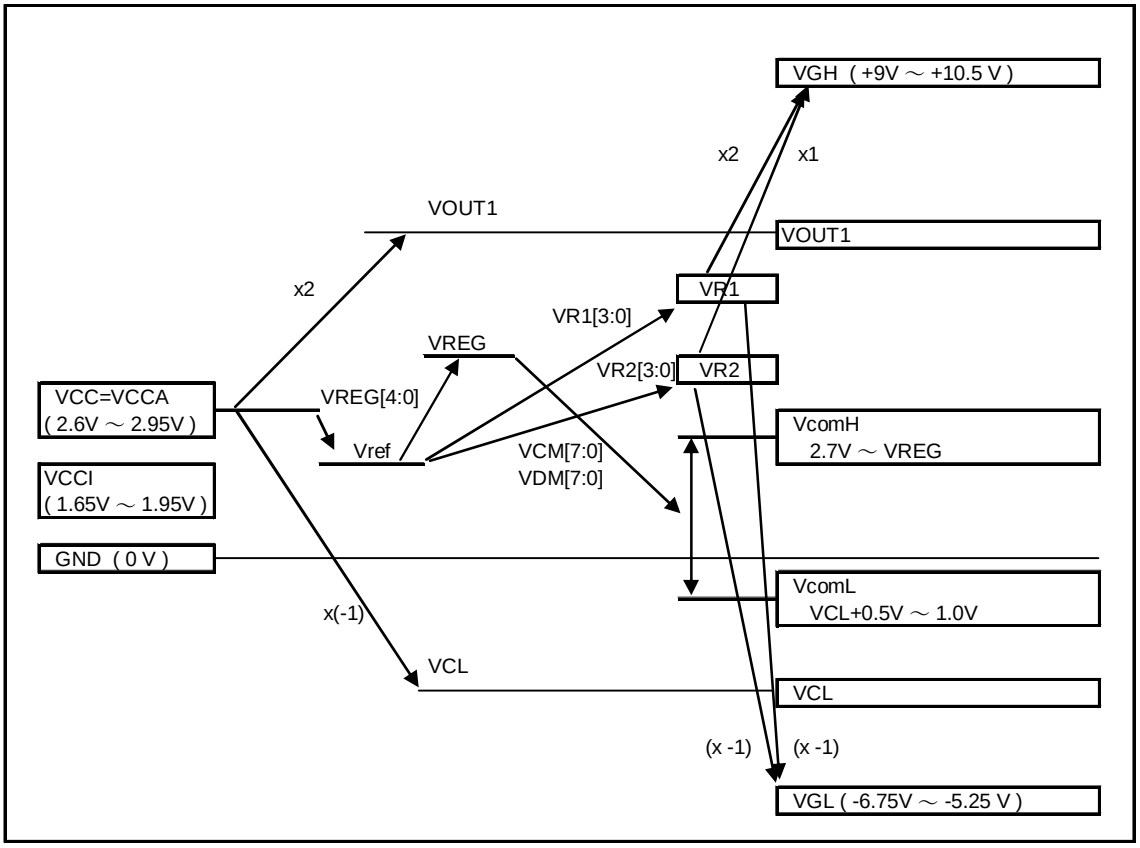


Fig6.1.2-1

6.1.3 VREG configuration

VREG shall be set lower than VOUT1-0.3V.

Register value					VREG output voltage (V)
VREG[4]	VREG[3]	VREG[2]	VREG[1]	VREG[0]	
0	0	0	0	0	Hi-Z
0	0	0	0	1	3.499
0	0	0	1	0	3.571
0	0	0	1	1	3.642
0	0	1	0	0	3.714
0	0	1	0	1	3.785
0	0	1	1	0	3.857
0	0	1	1	1	3.928
0	1	0	0	0	4.000
0	1	0	0	1	4.071
0	1	0	1	0	4.143
0	1	0	1	1	4.214
0	1	1	0	0	4.286
0	1	1	0	1	4.357
0	1	1	1	0	4.429
0	1	1	1	1	4.500
1	0	0	0	0	4.572
1	0	0	0	1	4.643
1	0	0	1	0	4.715
1	0	0	1	1	4.786
1	0	1	0	0	4.858
1	0	1	0	1	4.929
1	0	1	1	0	5.001
1	0	1	1	1	5.072
1	1	0	0	0	5.144
1	1	0	0	1	5.215
1	1	0	1	0	5.287
1	1	0	1	1	5.358
1	1	1	0	0	5.430
1	1	1	0	1	5.501
1	1	1	1	0	5.573
1	1	1	1	1	5.644

6.1.4 VR1 Regulator configuration

VR1 shall be set lower than VOUT1-0.5V..

Register value				VR1 output voltage (V)
VR1[3]	VR1[2]	VR1[1]	VR1[0]	
0	0	0	0	Hi-Z
0	0	0	1	2.838
0	0	1	0	2.970
0	0	1	1	3.102
0	1	0	0	3.234
0	1	0	1	3.366
0	1	1	0	3.498
0	1	1	1	3.630
1	0	0	0	3.762
1	0	0	1	3.894
1	0	1	0	4.026
1	0	1	1	4.158
1	1	0	0	4.290
1	1	0	1	4.422
1	1	1	0	4.554
1	1	1	1	4.686

6.1.5. VR2 Regulator configuration

VR2 shall be set lower than VOUT1-0.5V.

Register value				VR2 output voltage (V)
VR2[3]	VR2[2]	VR2[1]	VR2[0]	
0	0	0	0	Hi-Z
0	0	0	1	1.265
0	0	1	0	1.430
0	0	1	1	1.595
0	1	0	0	1.760
0	1	0	1	1.925
0	1	1	0	2.090
0	1	1	1	2.255
1	0	0	0	2.420
1	0	0	1	2.585
1	0	1	0	2.750
1	0	1	1	2.915
1	1	0	0	3.080
1	1	0	1	3.245
1	1	1	0	3.410
1	1	1	1	3.575

6.1.6. VGH and VGL configuration

VGH and VGL are set with VR1 and VR2.
Top column of each condition shows VGH.
Bottom column of each condition shows VGL.
Colored column meet target voltage.

		VR1 (V)														
		2.84	2.97	3.10	3.23	3.37	3.50	3.63	3.76	3.89	4.03	4.16	4.29	4.42	4.55	4.69
VR2 (V)	1.27	6.94	7.21	7.47	7.73	8.00	8.26	8.53	8.79	9.05	9.32	9.58	9.85	10.11	10.37	10.64
		-4.10	-4.24	-4.37	-4.50	-4.63	-4.76	-4.90	-5.03	-5.16	-5.29	-5.42	-5.56	-5.69	-5.82	-5.95
	1.43	7.11	7.37	7.63	7.90	8.16	8.43	8.69	8.95	9.22	9.48	9.75	10.01	10.27	10.54	10.80
		-4.27	-4.40	-4.53	-4.66	-4.80	-4.93	-5.06	-5.19	-5.32	-5.46	-5.59	-5.72	-5.85	-5.98	-6.12
	1.60	7.27	7.54	7.80	8.06	8.33	8.59	8.86	9.12	9.38	9.65	9.91	10.18	10.44	10.70	10.97
		-4.43	-4.57	-4.70	-4.83	-4.96	-5.09	-5.23	-5.36	-5.49	-5.62	-5.75	-5.89	-6.02	-6.15	-6.28
	1.76	7.44	7.70	7.96	8.23	8.49	8.76	9.02	9.28	9.55	9.81	10.08	10.34	10.60	10.87	11.13
		-4.60	-4.73	-4.86	-4.99	-5.13	-5.26	-5.39	-5.52	-5.65	-5.79	-5.92	-6.05	-6.18	-6.31	-6.45
	1.93	7.60	7.87	8.13	8.39	8.66	8.92	9.19	9.45	9.71	9.98	10.24	10.51	10.77	11.03	11.30
		-4.76	-4.90	-5.03	-5.16	-5.29	-5.42	-5.56	-5.69	-5.82	-5.95	-6.08	-6.22	-6.35	-6.48	-6.61
	2.09	7.77	8.03	8.29	8.56	8.82	9.09	9.35	9.61	9.88	10.14	10.41	10.67	10.93	11.20	11.46
		-4.93	-5.06	-5.19	-5.32	-5.46	-5.59	-5.72	-5.85	-5.98	-6.12	-6.25	-6.38	-6.51	-6.64	-6.78
	2.26	7.93	8.20	8.46	8.72	8.99	9.25	9.52	9.78	10.04	10.31	10.57	10.84	11.10	11.36	11.63
		-5.09	-5.23	-5.36	-5.49	-5.62	-5.75	-5.89	-6.02	-6.15	-6.28	-6.41	-6.55	-6.68	-6.81	-6.94
	2.42	8.10	8.36	8.62	8.89	9.15	9.42	9.68	9.94	10.21	10.47	10.74	11.00	11.26	11.53	11.79
		-5.26	-5.39	-5.52	-5.65	-5.79	-5.92	-6.05	-6.18	-6.31	-6.45	-6.58	-6.71	-6.84	-6.97	-7.11
	2.59	8.26	8.53	8.79	9.05	9.32	9.58	9.85	10.11	10.37	10.64	10.90	11.17	11.43	11.69	11.96
		-5.42	-5.56	-5.69	-5.82	-5.95	-6.08	-6.22	-6.35	-6.48	-6.61	-6.74	-6.88	-7.01	-7.14	-7.27
	2.75	8.43	8.69	8.95	9.22	9.48	9.75	10.01	10.27	10.54	10.80	11.07	11.33	11.59	11.86	12.12
		-5.59	-5.72	-5.85	-5.98	-6.12	-6.25	-6.38	-6.51	-6.64	-6.78	-6.91	-7.04	-7.17	-7.30	-7.44
	2.92	8.59	8.86	9.12	9.38	9.65	9.91	10.18	10.44	10.70	10.97	11.23	11.50	11.76	12.02	12.29
		-5.75	-5.89	-6.02	-6.15	-6.28	-6.41	-6.55	-6.68	-6.81	-6.94	-7.07	-7.21	-7.34	-7.47	-7.60
	3.08	8.76	9.02	9.28	9.55	9.81	10.08	10.34	10.60	10.87	11.13	11.40	11.66	11.92	12.19	12.45
		-5.92	-6.05	-6.18	-6.31	-6.45	-6.58	-6.71	-6.84	-6.97	-7.11	-7.24	-7.37	-7.50	-7.63	-7.77
	3.25	8.92	9.19	9.45	9.71	9.98	10.24	10.51	10.77	11.03	11.30	11.56	11.83	12.09	12.35	12.62
		-6.08	-6.22	-6.35	-6.48	-6.61	-6.74	-6.88	-7.01	-7.14	-7.27	-7.40	-7.54	-7.67	-7.80	-7.93
	3.41	9.09	9.35	9.61	9.88	10.14	10.41	10.67	10.93	11.20	11.46	11.73	11.99	12.25	12.52	12.78
		-6.25	-6.38	-6.51	-6.64	-6.78	-6.91	-7.04	-7.17	-7.30	-7.44	-7.57	-7.70	-7.83	-7.96	-8.10
	3.58	9.25	9.52	9.78	10.04	10.31	10.57	10.84	11.10	11.36	11.63	11.89	12.16	12.42	12.68	12.95
		-6.41	-6.55	-6.68	-6.81	-6.94	-7.07	-7.21	-7.34	-7.47	-7.60	-7.73	-7.87	-8.00	-8.13	-8.26

*** : VGH
*** : VGL

6.1.7. VCOM amplitude configuration

VCOM amplitude is defined with VDM and its calculation is as below.
VCOM amplitude = VREG x (0.6048+0.0021*VDM)
(Note) VCOML shall be higher than VCL+0.5V.
Please set VDM and VCM to meet above condition.)

HEX	VDM7	VDM6	VDM5	VDM4	VDM3	VDM2	VDM1	VDM0	VCOM amplitude
00'h	0	0	0	0	0	0	0	0	VREG X 0.6048
01'h	0	0	0	0	0	0	0	1	VREG X 0.6069
02'h	0	0	0	0	0	0	1	0	VREG X 0.6090
03'h	0	0	0	0	0	0	1	1	VREG X 0.6111
04'h	0	0	0	0	0	1	0	0	VREG X 0.6132
05'h	0	0	0	0	0	1	0	1	VREG X 0.6153
06'h	0	0	0	0	0	1	1	0	VREG X 0.6174
07'h	0	0	0	0	0	1	1	1	VREG X 0.6195
08'h	0	0	0	0	1	0	0	0	VREG X 0.6216
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
F7'h	1	1	1	1	0	1	1	1	VREG X 1.1235
F8'h	1	1	1	1	1	0	0	0	VREG X 1.1256
F9'h	1	1	1	1	1	0	0	1	VREG X 1.1277
FA'h	1	1	1	1	1	0	1	0	VREG X 1.1298
FB'h	1	1	1	1	1	0	1	1	VREG X 1.1319
FC'h	1	1	1	1	1	1	0	0	VREG X 1.1340
FD'h	1	1	1	1	1	1	0	1	VREG X 1.1361
FE'h	1	1	1	1	1	1	1	0	VREG X 1.1382
FF'h	1	1	1	1	1	1	1	1	VREG X 1.1403

Please, set VDM,VCM with below conditions

1) 2.7V < VCOMH < VREG
   VCOMH becomes VREG level when VCOMH setting level larger than VREG level.
   VCOMH<2.7V is setting disable. If VCOMH set smaller than 2.7V, it's AC and DC characteristics are outside of the grantee.
2) VCOML > VCL + 0.5V
   If VCOML>VCL+0.5V, VCOML's AC and DC characteristics are outside of the grantee as same to above VCOMH(VCOMH<2.7V).

6.1.8. VCOM center configuration

VCOM center value is defined with VCM and its calculation is as below.
VCOM center = VREG x (0.23455+0.00105*VCM)
(Note) VCOML shall be higher than VCL+0.5V.
Please set VDM and VCM to meet above condition.)

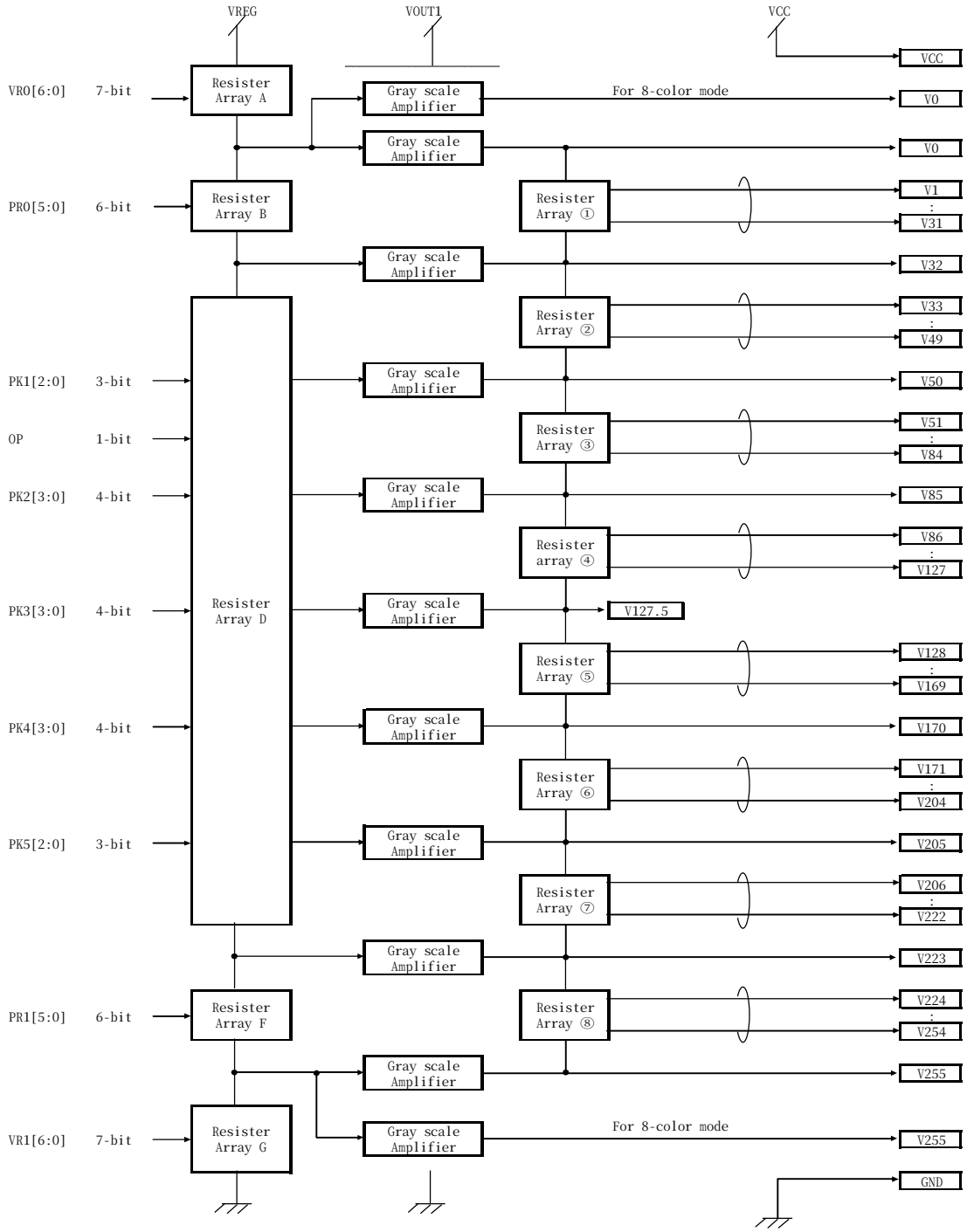
HEX	VCM7	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOM center voltage
00'h	0	0	0	0	0	0	0	0	VREG X 0.23455
01'h	0	0	0	0	0	0	0	1	VREG X 0.23560
02'h	0	0	0	0	0	0	1	0	VREG X 0.23665
03'h	0	0	0	0	0	0	1	1	VREG X 0.23770
04'h	0	0	0	0	0	1	0	0	VREG X 0.23875
05'h	0	0	0	0	0	1	0	1	VREG X 0.23980
06'h	0	0	0	0	0	1	1	0	VREG X 0.24085
07'h	0	0	0	0	0	1	1	1	VREG X 0.24190
08'h	0	0	0	0	1	0	0	0	VREG X 0.24295
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
F7'h	1	1	1	1	0	1	1	1	VREG X 0.49390
F8'h	1	1	1	1	1	0	0	0	VREG X 0.49495
F9'h	1	1	1	1	1	0	0	1	VREG X 0.49600
FA'h	1	1	1	1	1	0	1	0	VREG X 0.49705
FB'h	1	1	1	1	1	0	1	1	VREG X 0.49810
FC'h	1	1	1	1	1	1	0	0	VREG X 0.49915
FD'h	1	1	1	1	1	1	0	1	VREG X 0.50020
FE'h	1	1	1	1	1	1	1	0	VREG X 0.50125
FF'h	1	1	1	1	1	1	1	1	VREG X 0.50230

Please, set VDM,VCM with below conditions

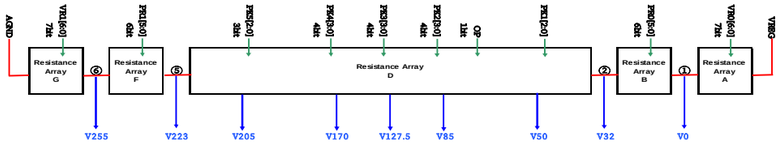
2) 2.7V < VCOMH < VREG
VCOMH becomes VREG level when VCOMH setting level larger than VREG level.
VCOMH<2.7V is setting disable. If VCOMH set smaller than 2.7V, it's AC and DC characteristics are outside of the grantee.

2) VCOML > VCL + 0.5V
If VCOML>VCL+0.5V, VCOML's AC and DC characteristics are outside of the grantee as same to above VCOMH(VCOMH<2.7V).

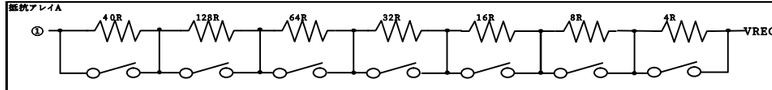
6.2 Gray Scale generation circuit
6.2.1. Block diagram



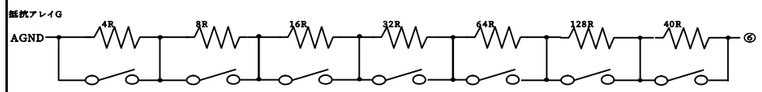
6.2.2. Resistance Array-1



抵抗アレイA



抵抗アレイG



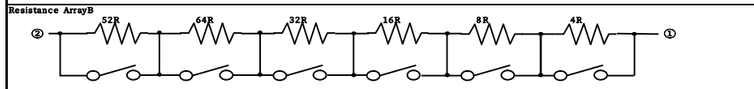
VR0/1[6:0]	VREG-Ⓐ/ AGND-Ⓑ Number of R
0 0 0 0 0 0 0	0 R
0 0 0 0 0 0 1	4 R
0 0 0 0 0 1 0	8 R
0 0 0 0 0 1 1	12 R
0 0 0 0 1 0 0	16 R
0 0 0 0 1 0 1	20 R
0 0 0 0 1 1 0	24 R
0 0 0 0 1 1 1	28 R
0 0 0 1 0 0 0	32 R
0 0 0 1 0 0 1	36 R
0 0 0 1 0 1 0	40 R
0 0 0 1 0 1 1	44 R
0 0 0 1 1 0 0	48 R
0 0 0 1 1 0 1	52 R
0 0 0 1 1 1 0	56 R
0 0 0 1 1 1 1	60 R
0 0 1 0 0 0 0	64 R
0 0 1 0 0 0 1	68 R
0 0 1 0 0 1 0	72 R
0 0 1 0 0 1 1	76 R
0 0 1 0 1 0 0	80 R
0 0 1 0 1 0 1	84 R
0 0 1 0 1 1 0	88 R
0 0 1 0 1 1 1	92 R
0 0 1 1 0 0 0	96 R
0 0 1 1 0 0 1	100 R
0 0 1 1 0 1 0	104 R
0 0 1 1 0 1 1	108 R
0 0 1 1 1 0 0	112 R
0 0 1 1 1 0 1	116 R
0 0 1 1 1 1 0	120 R
0 0 1 1 1 1 1	124 R

VR0/1[6:0]	VREG-Ⓐ/ AGND-Ⓑ Number of R
0 1 0 0 0 0 0	128 R
0 1 0 0 0 0 1	132 R
0 1 0 0 0 1 0	136 R
0 1 0 0 0 1 1	140 R
0 1 0 0 1 0 0	144 R
0 1 0 0 1 0 1	148 R
0 1 0 0 1 1 0	152 R
0 1 0 0 1 1 1	156 R
0 1 0 1 0 0 0	160 R
0 1 0 1 0 0 1	164 R
0 1 0 1 0 1 0	168 R
0 1 0 1 0 1 1	172 R
0 1 0 1 1 0 0	176 R
0 1 0 1 1 0 1	180 R
0 1 0 1 1 1 0	184 R
0 1 0 1 1 1 1	188 R
0 1 1 0 0 0 0	192 R
0 1 1 0 0 0 1	196 R
0 1 1 0 0 1 0	200 R
0 1 1 0 0 1 1	204 R
0 1 1 0 1 0 0	208 R
0 1 1 0 1 0 1	212 R
0 1 1 0 1 1 0	216 R
0 1 1 0 1 1 1	220 R
0 1 1 1 0 0 0	224 R
0 1 1 1 0 0 1	228 R
0 1 1 1 0 1 0	232 R
0 1 1 1 0 1 1	236 R
0 1 1 1 1 0 0	240 R
0 1 1 1 1 0 1	244 R
0 1 1 1 1 1 0	248 R
0 1 1 1 1 1 1	252 R

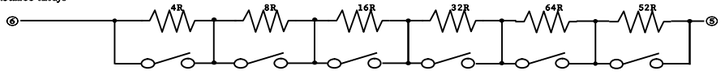
VR0/1[6:0]	VREG-Ⓐ/ AGND-Ⓑ Number of R
1 0 0 0 0 0 0	40 R
1 0 0 0 0 0 1	44 R
1 0 0 0 0 1 0	48 R
1 0 0 0 0 1 1	52 R
1 0 0 0 1 0 0	56 R
1 0 0 0 1 0 1	60 R
1 0 0 0 1 1 0	64 R
1 0 0 0 1 1 1	68 R
1 0 0 1 0 0 0	72 R
1 0 0 1 0 0 1	76 R
1 0 0 1 0 1 0	80 R
1 0 0 1 0 1 1	84 R
1 0 0 1 1 0 0	88 R
1 0 0 1 1 0 1	92 R
1 0 0 1 1 1 0	96 R
1 0 0 1 1 1 1	100 R
1 0 1 0 0 0 0	104 R
1 0 1 0 0 0 1	108 R
1 0 1 0 0 1 0	112 R
1 0 1 0 0 1 1	116 R
1 0 1 0 1 0 0	120 R
1 0 1 0 1 0 1	124 R
1 0 1 0 1 1 0	128 R
1 0 1 0 1 1 1	132 R
1 0 1 1 0 0 0	136 R
1 0 1 1 0 0 1	140 R
1 0 1 1 0 1 0	144 R
1 0 1 1 0 1 1	148 R
1 0 1 1 1 0 0	152 R
1 0 1 1 1 0 1	156 R
1 0 1 1 1 1 0	160 R
1 0 1 1 1 1 1	164 R

VR0/1[6:0]	VREG-Ⓐ/ AGND-Ⓑ Number of R
1 1 0 0 0 0 0	168 R
1 1 0 0 0 0 1	172 R
1 1 0 0 0 1 0	176 R
1 1 0 0 0 1 1	180 R
1 1 0 0 1 0 0	184 R
1 1 0 0 1 0 1	188 R
1 1 0 0 1 1 0	192 R
1 1 0 0 1 1 1	196 R
1 1 0 1 0 0 0	200 R
1 1 0 1 0 0 1	204 R
1 1 0 1 0 1 0	208 R
1 1 0 1 0 1 1	212 R
1 1 0 1 1 0 0	216 R
1 1 0 1 1 0 1	220 R
1 1 0 1 1 1 0	224 R
1 1 0 1 1 1 1	228 R
1 1 1 0 0 0 0	232 R
1 1 1 0 0 0 1	236 R
1 1 1 0 0 1 0	240 R
1 1 1 0 0 1 1	244 R
1 1 1 0 1 0 0	248 R
1 1 1 0 1 0 1	252 R
1 1 1 0 1 1 0	256 R
1 1 1 0 1 1 1	260 R
1 1 1 1 0 0 0	264 R
1 1 1 1 0 0 1	268 R
1 1 1 1 0 1 0	272 R
1 1 1 1 0 1 1	276 R
1 1 1 1 1 0 0	280 R
1 1 1 1 1 0 1	284 R
1 1 1 1 1 1 0	288 R
1 1 1 1 1 1 1	292 R

Resistance ArrayB



Resistance ArrayF



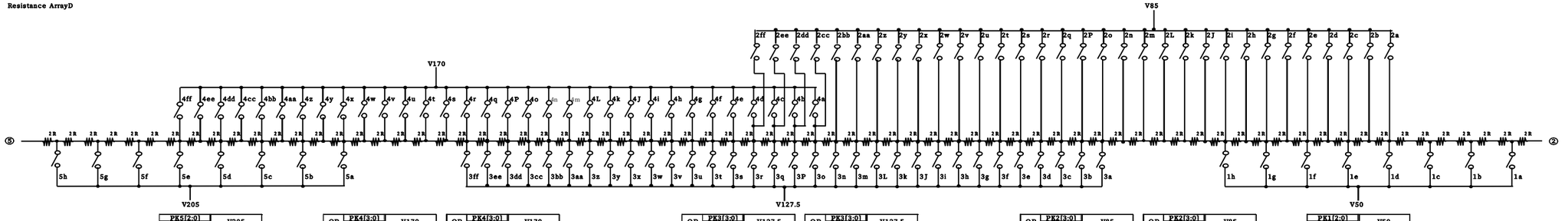
FR0[5:0]	Ⓐ-Ⓑ Number of R
0 0 0 0 0 0	0 R
0 0 0 0 0 1	4 R
0 0 0 0 1 0	8 R
0 0 0 0 1 1	12 R
0 0 0 1 0 0	16 R
0 0 0 1 0 1	20 R
0 0 0 1 1 0	24 R
0 0 0 1 1 1	28 R
0 0 1 0 0 0	32 R
0 0 1 0 0 1	36 R
0 0 1 0 1 0	40 R
0 0 1 0 1 1	44 R
0 0 1 1 0 0	48 R
0 0 1 1 0 1	52 R
0 0 1 1 1 0	56 R
0 0 1 1 1 1	60 R
0 1 0 0 0 0	64 R
0 1 0 0 0 1	68 R
0 1 0 0 1 0	72 R
0 1 0 0 1 1	76 R
0 1 0 1 0 0	80 R
0 1 0 1 0 1	84 R
0 1 0 1 1 0	88 R
0 1 0 1 1 1	92 R
0 1 1 0 0 0	96 R
0 1 1 0 0 1	100 R
0 1 1 0 1 0	104 R
0 1 1 0 1 1	108 R
0 1 1 1 0 0	112 R
0 1 1 1 0 1	116 R
0 1 1 1 1 0	120 R
0 1 1 1 1 1	124 R

FR0[5:0]	Ⓐ-Ⓑ Number of R
1 0 0 0 0 0	52 R
1 0 0 0 0 1	56 R
1 0 0 0 1 0	60 R
1 0 0 0 1 1	64 R
1 0 0 1 0 0	68 R
1 0 0 1 0 1	72 R
1 0 0 1 1 0	76 R
1 0 0 1 1 1	80 R
1 0 1 0 0 0	84 R
1 0 1 0 0 1	88 R
1 0 1 0 1 0	92 R
1 0 1 0 1 1	96 R
1 0 1 1 0 0	100 R
1 0 1 1 0 1	104 R
1 0 1 1 1 0	108 R
1 0 1 1 1 1	112 R
1 1 0 0 0 0	116 R
1 1 0 0 0 1	120 R
1 1 0 0 1 0	124 R
1 1 0 0 1 1	128 R
1 1 0 1 0 0	132 R
1 1 0 1 0 1	136 R
1 1 0 1 1 0	140 R
1 1 0 1 1 1	144 R
1 1 1 0 0 0	148 R
1 1 1 0 0 1	152 R
1 1 1 0 1 0	156 R
1 1 1 0 1 1	160 R
1 1 1 1 0 0	164 R
1 1 1 1 0 1	168 R
1 1 1 1 1 0	172 R
1 1 1 1 1 1	176 R

FR1[5:0]	Ⓐ-Ⓑ Number of R
0 0 0 0 0 0	0 R
0 0 0 0 0 1	4 R
0 0 0 0 1 0	8 R
0 0 0 0 1 1	12 R
0 0 0 1 0 0	16 R
0 0 0 1 0 1	20 R
0 0 0 1 1 0	24 R
0 0 0 1 1 1	28 R
0 0 1 0 0 0	32 R
0 0 1 0 0 1	36 R
0 0 1 0 1 0	40 R
0 0 1 0 1 1	44 R
0 0 1 1 0 0	48 R
0 0 1 1 0 1	52 R
0 0 1 1 1 0	56 R
0 0 1 1 1 1	60 R
0 1 0 0 0 0	64 R
0 1 0 0 0 1	68 R
0 1 0 0 1 0	72 R
0 1 0 0 1 1	76 R
0 1 0 1 0 0	80 R
0 1 0 1 0 1	84 R
0 1 0 1 1 0	88 R
0 1 0 1 1 1	92 R
0 1 1 0 0 0	96 R
0 1 1 0 0 1	100 R
0 1 1 0 1 0	104 R
0 1 1 0 1 1	108 R
0 1 1 1 0 0	112 R
0 1 1 1 0 1	116 R
0 1 1 1 1 0	120 R
0 1 1 1 1 1	124 R

FR1[5:0]	Ⓐ-Ⓑ Number of R
1 0 0 0 0 0	52 R
1 0 0 0 0 1	56 R
1 0 0 0 1 0	60 R
1 0 0 0 1 1	64 R
1 0 0 1 0 0	68 R
1 0 0 1 0 1	72 R
1 0 0 1 1 0	76 R
1 0 0 1 1 1	80 R
1 0 1 0 0 0	84 R
1 0 1 0 0 1	88 R
1 0 1 0 1 0	92 R
1 0 1 0 1 1	96 R
1 0 1 1 0 0	100 R
1 0 1 1 0 1	104 R
1 0 1 1 1 0	108 R
1 0 1 1 1 1	112 R
1 1 0 0 0 0	116 R
1 1 0 0 0 1	120 R
1 1 0 0 1 0	124 R
1 1 0 0 1 1	128 R
1 1 0 1 0 0	132 R
1 1 0 1 0 1	136 R
1 1 0 1 1 0	140 R
1 1 0 1 1 1	144 R
1 1 1 0 0 0	148 R
1 1 1 0 0 1	152 R
1 1 1 0 1 0	156 R
1 1 1 0 1 1	160 R
1 1 1 1 0 0	164 R
1 1 1 1 0 1	168 R
1 1 1 1 1 0	172 R
1 1 1 1 1 1	176 R

Resistance ArrayD



PK5[2:0]	V205
0 0 0	5a
0 0 1	5b
0 1 0	5c
0 1 1	5d
1 0 0	5e
1 0 1	5f
1 1 0	5g
1 1 1	5h

OP	PK4[3:0]	V170
0	0 0 0 0	4a
0	0 0 0 1	4b
0	0 0 1 0	4c
0	0 0 1 1	4d
0	0 1 0 0	4e
0	0 1 0 1	4f
0	0 1 1 0	4g
0	0 1 1 1	4h
0	1 0 0 0	4i
0	1 0 0 1	4J
0	1 0 1 0	4k
0	1 0 1 1	4L
0	1 1 0 0	4m
0	1 1 0 1	4n
0	1 1 1 0	4o
0	1 1 1 1	4p

OP	PK4[3:0]	V170
1	0 0 0 0	4q
1	0 0 0 1	4r
1	0 0 1 0	4s
1	0 0 1 1	4t
1	0 1 0 0	4u
1	0 1 0 1	4v
1	0 1 1 0	4w
1	0 1 1 1	4x
1	1 0 0 0	4y
1	1 0 0 1	4z
1	1 0 1 0	4aa
1	1 0 1 1	4bb
1	1 1 0 0	4cc
1	1 1 0 1	4dd
1	1 1 1 0	4ee
1	1 1 1 1	4ff

OP	PK3[3:0]	V127.5
0	0 0 0 0	3a
0	0 0 0 1	3b
0	0 0 1 0	3c
0	0 0 1 1	3d
0	0 1 0 0	3e
0	0 1 0 1	3f
0	0 1 1 0	3g
0	0 1 1 1	3h
0	1 0 0 0	3i
0	1 0 0 1	3J
0	1 0 1 0	3k
0	1 0 1 1	3l
0	1 1 0 0	3m
0	1 1 0 1	3n
0	1 1 1 0	3o
0	1 1 1 1	3p

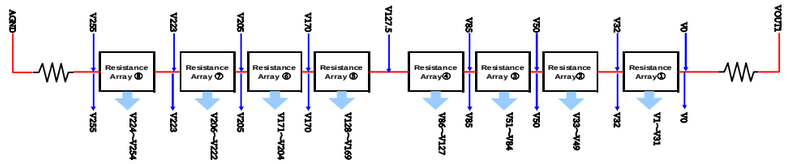
OP	PK3[3:0]	V127.5
1	0 0 0 0	3q
1	0 0 0 1	3r
1	0 0 1 0	3s
1	0 0 1 1	3t
1	0 1 0 0	3u
1	0 1 0 1	3v
1	0 1 1 0	3w
1	0 1 1 1	3x
1	1 0 0 0	3y
1	1 0 0 1	3z
1	1 0 1 0	3aa
1	1 0 1 1	3bb
1	1 1 0 0	3cc
1	1 1 0 1	3dd
1	1 1 1 0	3ee
1	1 1 1 1	3ff

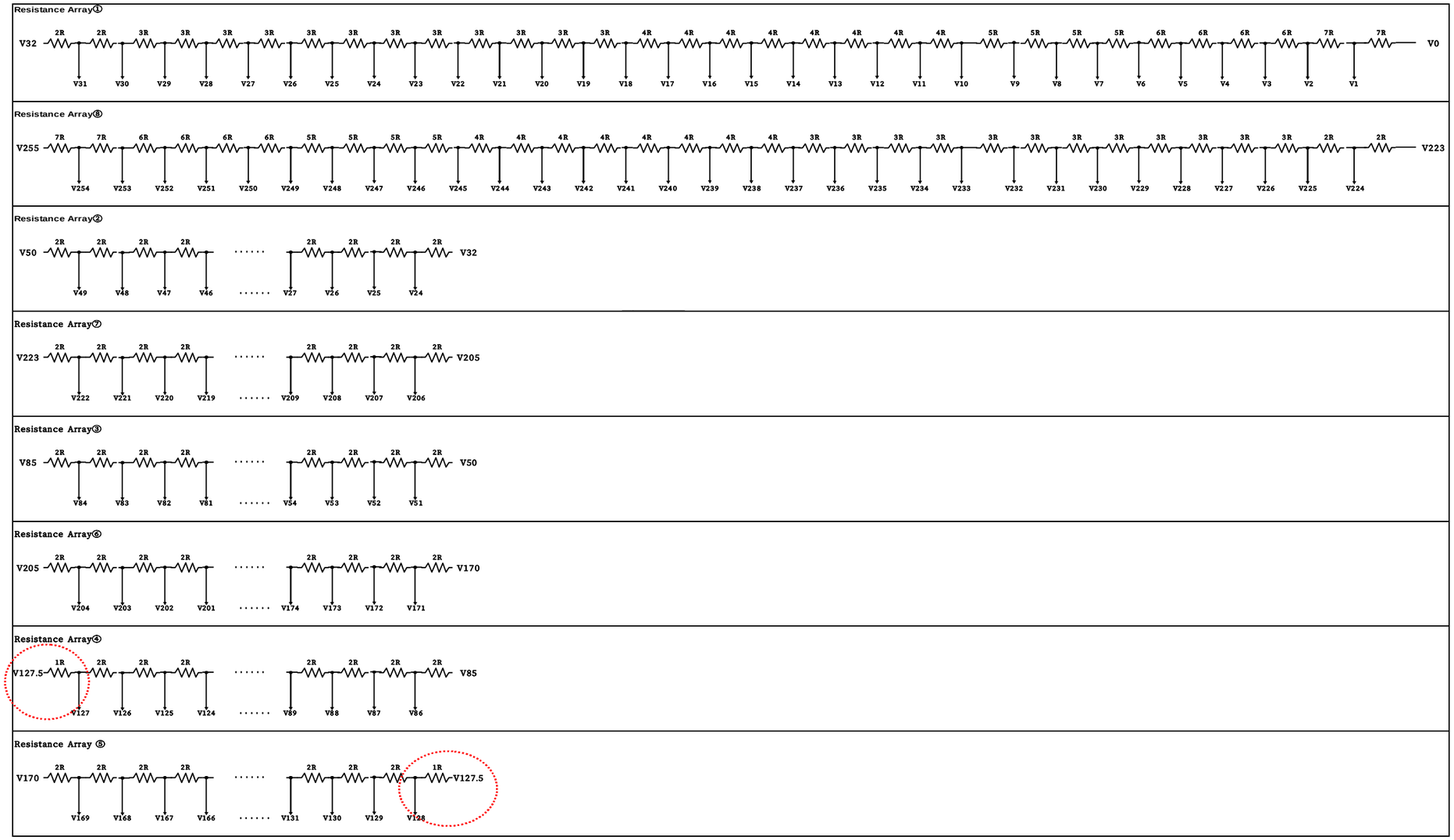
OP	PK2[3:0]	V85
0	0 0 0 0	2a
0	0 0 0 1	2b
0	0 0 1 0	2c
0	0 0 1 1	2d
0	0 1 0 0	2e
0	0 1 0 1	2f
0	0 1 1 0	2g
0	0 1 1 1	2h
0	1 0 0 0	2i
0	1 0 0 1	2J
0	1 0 1 0	2k
0	1 0 1 1	2L
0	1 1 0 0	2m
0	1 1 0 1	2n
0	1 1 1 0	2o
0	1 1 1 1	2p

OP	PK2[3:0]	V85
1	0 0 0 0	2q
1	0 0 0 1	2r
1	0 0 1 0	2s
1	0 0 1 1	2t
1	0 1 0 0	2u
1	0 1 0 1	2v
1	0 1 1 0	2w
1	0 1 1 1	2x
1	1 0 0 0	2y
1	1 0 0 1	2z
1	1 0 1 0	2aa
1	1 0 1 1	2bb
1	1 1 0 0	2cc
1	1 1 0 1	2dd
1	1 1 1 0	2ee
1	1 1 1 1	2ff

PK1[2:0]	V50
0 0 0	1a
0 0 1	1b
0 1 0	1c
0 1 1	1d
1 0 0	1e
1 0 1	1f
1 1 0	1g
1 1 1	1h

6.2.3. Resistance Array-2





7.Command

7.1.Command List

Operational Code	Function	Read/ Write/ Command	Number Of Parameter	Parameters
00	No Operation	C	0	
01	Software reset	C	0	
04	Read Display Identification Information	R	4	
09	Read Display Status	R	5	
0A	Read Display Power Mode	R	1	
0B	Read Display MADCTL	R	1	
0C	Read Display Pixel Format	R	1	
0D	Read Display Image Mode	R	1	
0E	Read Display Signal Mode	R	1	
0F	Read Display Self Diagnostic Result	R	1	
10	Sleep in	C	0	
11	Sleep out	C	0	
12	Partial Mode On	C	0	
13	Normal Display Mode On	C	0	
20	Display Inversion off	C	0	
21	Display Inversion on	C	0	
26	Gamma Set	W	1	format: 1 byte for curve selection
28	Display off	C	0	
29	Display on	C	0	
2A	Column Address Set	W	4	format: 2 bytes for leftmost Column counter 2 bytes for rightmost Column counter
2B	Page Address Set	W	4	format: 2 bytes for top line pointer 2 bytes for bottom line pointer

Operational Code	Function	Read/ Write/ Command	Number Of Parameter	Parameters
2C	Memory Write	W	Any length	Successive video data stream format: In 4,096 colour mode (16/8X = High), Phase 1 D[15...0]=R[3..0]G[3..0]B[3..0] Phase 2 D[15...0]=R[3..0]G[3..0]B[3..0] In 64k colour mode (16/8X = High), Phase 1 D[15...0]=R[4..0]G[5..0]B[4..0] Phase 2 D[15...0]=R[4..0]G[5..0]B[4..0] In 262k colour mode (16/8X = High), Phase 1 D[15...0]=R[5..0]G[5..0] Phase 2 D[15...0]=B[5..0]R[5..0] Phase 3 D[15...0]=G[5..0]B[5..0] In 16.7M colour mode (16/8X = High), Phase 1 D[15...0]=R[7..0]G[7..0] Phase 2 D[15...0]=B[7..0]R[7..0] Phase 3 D[15...0]=G[7..0]B[7..0] In 4,096 colour mode (16/8X = Low), Phase 1 D[7...0]=R[3..0]G[3..0] Phase 2 D[7...0]=B[3..0]R[3..0] Phase 3 D[7...0]=G[3..0]B[3..0] In 64k colour mode (16/8X = Low), Phase 1 D[7...0]=R[4..0]G[5..3] Phase 2 D[7...0]=G[2..0]B[4..0] In 262k colour mode (16/8X = Low), Phase 1 D[7...0]=R[5..0] Phase 2 D[7...0]=G[5..0] Phase 3 D[7...0]=B[5..0] In 16.7M colour mode (16/8X = Low), Phase 1 D[7...0]=R[7..0] Phase 2 D[7...0]=G[7..0] Phase 3 D[7...0]=B[7..0]
2D	Colour set	W	192	format: 64 bytes for R, G and B colours to be stored in the look-up table
2E	Memory Read	R	Any length	Successive video data stream Format in all colour modes (16/8X = High), Phase 1 D[15..0]=R[7..0]G[7..0] Phase 2 D[15..0]=B[7..0]R[7..0] Phase 3 D[15..0]=G[7..0]B[7..0] Format in all colour modes (16/8X = Low), Phase 1 D[15..0]=R[7..0] Phase 2 D[15..0]=G[7..0] Phase 3 D[15..0]=B[7..0]

Operational Code	Function	Read/ Write/ Command	Number Of Parameter	Parameters
30	Partial area	W	4	format: 2 byte for top line pointer 2 byte for bottom line pointer
33	Vertical Scrolling Definition	W	6	format: 2 byte for fixed area top line pointer 2 byte for scrolling area height 2 byte for fixed area bottom line pointer
34	Tearing Effect Line Off	C	0	
35	Tearing Effect Line On	W	1	1 byte for Tearing Effect Line Mode selection.
36	Memory Access Control	W	1	1 byte for memory scan direction
37	Vertical scrolling start Address	W	2	2 byte for line pointer
38	Idle Mode off	C	0	-
39	Idle Mode on	C	0	-
3A	Interface pixel format	W	1	Please Refer to Table in Section 9.2.33.
DA	Read ID1	R	(1)	xx for xx Corporation
DB	Read ID2	R	(1)	format: 128 to 255 for module version.
DC	Read ID3	R	(1)	xx for this project.

Note 1: Undefined commands are treated as NOP (00H) command.

Note 2: B0 to D9 and DE to FF are for factory use of display supplier. Default value is NOP(00H).

Note 3: Commands 10H, 12H, 13H, 20H, 21H, 26H, 28H, 29H, 30H, 33H, 36H (Bit B4 only), 37H, 38H and 39H are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09H), Read Display Power Mode (0AH), Read Display MADCTL (0BH), Read Display Pixel Format (0CH), Read Display Image Mode (0DH), Read Display Signal Mode (0EH) and Read Display Self Diagnostic Result (0FH) of these commands is updated immediately both in Sleep In mode and Sleep Out mode.

7.2. Command Description

7.2.1. NOP (00h)

<table>
<tr><th>00 H</th><th colspan="19">NOP (No Operation)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>B15</td><td>B14</td><td>B13</td><td>B12</td><td>B11</td><td>B10</td><td>B9</td><td>B8</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Parameter</td><td colspan="20">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="20">This command is an empty command; it does not have any effect on the display module.
However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.

X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="20"></td></tr>
<tr><td>Register Availability</td><td colspan="20"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="20"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="20"></td></tr>
</table>

7.2.2. Software Reset (01h)

01 H	SWRESET (Software Reset)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	1	01
Parameter	NO PARAMETER																			
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are unaffected by this command X = don't care.																			
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier's factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.																			

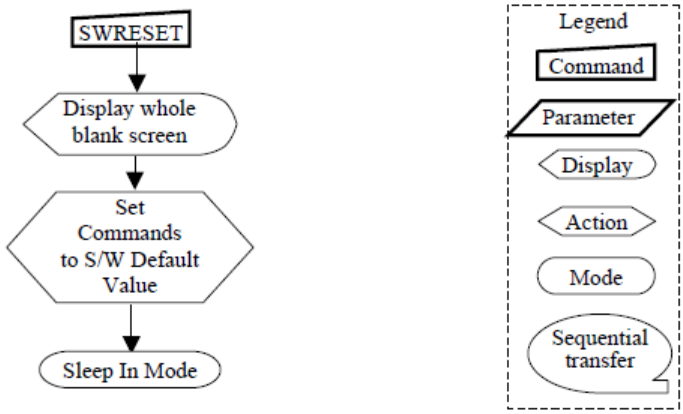
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A

Flow Chart



7.2.3. Read Display Identification Information (04h)

04 H	RDDIDIF (Read Display Identification Information)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	0	0	0	1	0	0	04
1st parameter	1	↑	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
2nd parameter	1	↑	1	X	X	X	X	X	X	X	X	xx	xx	xx	xx	xx	xx	xx	xx	xx
3rd parameter	1	↑	1	X	X	X	X	X	X	X	X	1	V6	V5	V4	V3	V2	V1	V0	80 … FF
4th parameter	1	↑	1	X	X	X	X	X	X	X	X	xx	xx	xx	xx	xx	xx	xx	xx	xx

Description

This read byte returns 24-bit display identification information.
The 1st Parameter is dummy read.
The 2nd Parameter identifies the LCD module's manufacturer.
The 3rd Parameter has 2 purposes. Bit7 (MSB) defines the type of panel. 0=Driver (STN B/W), 1=Module (Colour). Bits 6..0 are used to track the LCD module/driver version. It is defined by display supplier (with end customer's agreement) and it changes each time a revision is made to the display, material or construction specifications. See Table:

ID Byte Value V[7…0]	Version	Changes
80h		
81h		
82h		
83h		

The 4th parameter identifies the LCD module/driver.
X = Don't care.

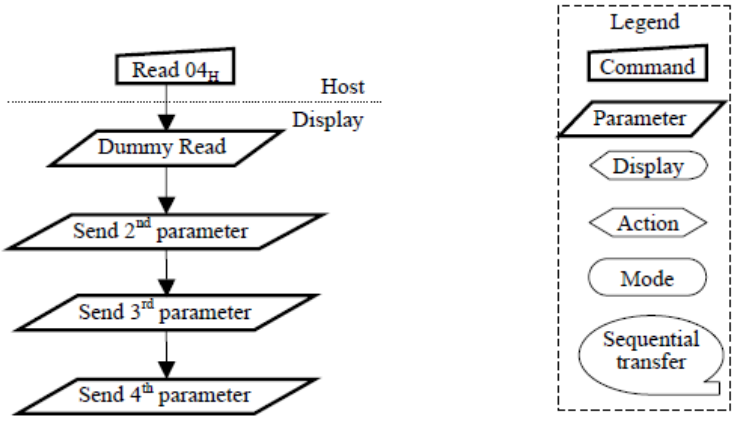
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	See Description
SW Reset	See Description
HW Reset	See Description

Flow Chart	

Read 04H
Host
Display
Dummy Read
Send 2nd parameter
Send 3rd parameter
Send 4th parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

7.2.4. Read Display Status (09h)

09 H	RDDST (Read Display Status)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	0	0	1	0	0	1	09
1st parameter	1	↑	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
2nd parameter	1	↑	1	X	X	X	X	X	X	X	X	D 31	D 30	D 29	D 28	D 27	D 26	D 25	0	xx
3rd parameter	1	↑	1	X	X	X	X	X	X	X	X	0	D 22	D 21	D 20	D 19	D 18	D 17	D 16	xx
4th parameter	1	↑	1	X	X	X	X	X	X	X	X	D 15	0	D 13	0	0	D 10	D 9	D 8	xx
5th parameter	1	↑	1	X	X	X	X	X	X	X	X	D 7	D 6	D 5	0	0	0	0	0	xx

Description

This command indicates the current status of the display as described in the table below: -

Bit	Description	Comment	Bit	Description	Comment
31	Booster Voltage Status		15	Vertical Scrolling Status	
30	Page Address Order		14	Horizontal Scrolling Status	Set to '0'
29	Column Address Order		13	Inversion Status	
28	Page/Column Order		12	All Pixels On	Set to '0'
27	Vertical Order		11	All Pixels Off	Set to '0'
26	RGB/BGR Order		10	Display On/Off	
25	Horizontal Order		9	Tearing Effect On/Off	
24	Switching between Segment outputs and RAM	Set to '0'	8	Gamma Curve Selection	
23	Switching between Common outputs and RAM	Set to '0'	7		
22	Interface Colour Pixel Format Definition		6		
21			5	Tearing Effect Output Line Mode	
20			4	For Future Use	Set to '0'
19	Idle Mode On/Off		3	For Future Use	Set to '0'
18	Partial Mode On/Off		2	For Future Use	Set to '0'
17	Sleep In/Out		1	For Future Use	Set to '0'
16	Display Normal Mode On/Off		0	For Future Use	Set to '0'

- Bit D31 – Booster Voltage Status
  '0' = Booster Off.
  '1' = Booster On.
- Bit D30 – Page Address Order
  '0' = Top to Bottom (When MADCTL B7='0').
  '1' = Bottom to Top (When MADCTL B7='1').
- Bit D29 – Column Address Order
  '0' = Left to Right (When MADCTL B6='0').
  '1' = Right to Left (When MADCTL B6='1').
- Bit D28 - Page/Column Order
  '0' = Normal Mode (When MADCTL B5='0').
  '1' = Reverse Mode (When MADCTL B5='1').

Note: For Bits D30 to D28, also refer to Section 8.2.3.

Description

- Bit D27 – Line Address Order
  '0' = LCD Refresh Top to Bottom (When MADCTL B4='0').
  '1' = LCD Refresh Bottom to Top (When MADCTL B4='1').
- Bit D26 – RGB/BGR Order
  '0' = RGB (When MADCTL B3='0').
  '1' = BGR (When MADCTL B3='1').
- Bit D25 – Display Data Latch Data Order (if this bit is not available, so it is set to '0')
  '0' = LCD Refresh Left to Right (When MADCTL B2='0').
  '1' = LCD Refresh Right to Left (When MADCTL B2='1').

Note: For Bits D27, D26, D25, also refer to Section 9.2.29.

- Bit D24 – Switching Between Segment Outputs and RAM
  This bit is not applicable for this project, so it is set to '0'
- Bit D23 – Switching Between Common Outputs and RAM
  This bit is not applicable for this project, so it is set to '0'
- Bits D22, D21, D20 – Interface Colour Pixel Format Definition

Interface Format	D22	D21	D20
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
12 bit/pixel	0	1	1
Not Defined	1	0	0
16 bit/pixel	1	0	1
18 bit/pixel	1	1	0
24 bit/pixel	1	1	1

- Bit D19 – Idle Mode On/Off
  '0' = Idle Mode Off.
  '1' = Idle Mode On.
- Bit D18 – Partial Mode On/Off
  '0' = Partial Mode Off.
  '1' = Partial Mode On.
- Bit D17 – Sleep In/Out
  '0' = Sleep In Mode.
  '1' = Sleep Out Mode.
- Bit D16 – Display Normal Mode On/Off
  '0' = Display Normal Mode Off.
  '1' = Display Normal Mode On.
- Bit D15 – Vertical Scrolling On/Off
  '0' = Vertical Scrolling is Off.
  '1' = Vertical Scrolling is On.
- Bit D14 – Horizontal Scrolling Status
  This bit is not applicable for this project, so it is set to '0'
- Bit D13 – Inversion On/Off
  '0' = Inversion is Off.
  '1' = Inversion is On.

Description

- Bit D12 – All Pixels On
  This bit is not applicable for this project, so it is set to '0'
- Bit D11 – All Pixels Off
  This bit is not applicable for this project, so it is set to '0'
- Bit D10 – Display On/Off
  '0' = Display is Off.
  '1' = Display is On.
- Bit D9 – Tearing Effect Line On/Off
  '0' =Tearing Effect Line Off.
  '1' = Tearing Effect On.
- Bits D8, D7, D6 – Gamma Curve Selection

Gamma Curve Selection	D8	D7	D6	Gamma Set (26h) Parameter
Gamma Curve 1	0	0	0	GC0
Gamma Curve 2	0	0	1	GC1
Gamma Curve 3	0	1	0	GC2
Gamma Curve 4	0	1	1	GC3
Not Defined	1	0	0	Not Defined
Not Defined	1	0	1	Not Defined
Not Defined	1	1	0	Not Defined
Not Defined	1	1	1	Not Defined

- Bit D5 – Tearing Effect Line Output Mode.
  '0' = Mode 1, V-Blanking only.
  '1' = Mode 2, both H-Blanking and V-Blanking.
- Bits D4, D3, D2, D1, D0 are for future use and are set to '0'.

X = Don't care

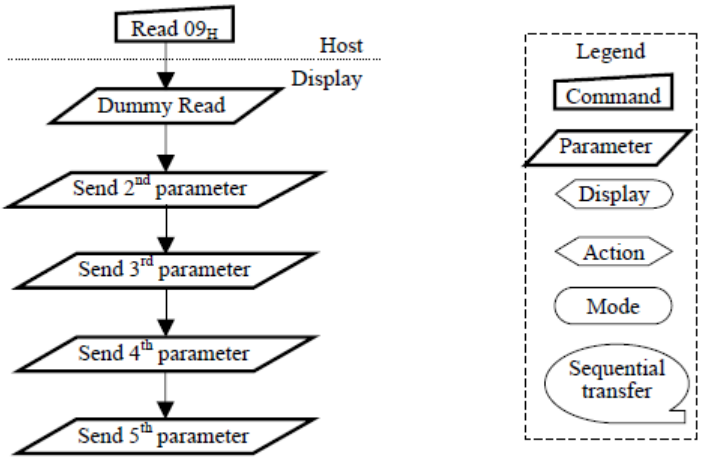
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	See Description
SW Reset	See Description
HW Reset	See Description

Flow Chart	

Read 09H
Host
Display
Dummy Read
Send 2nd parameter
Send 3rd parameter
Send 4th parameter
Send 5th parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

7.2.5. Read Display Power Mode (0Ah)

<table>
<tr><th>0A H</th><th colspan="19">RDDPM (Read Display Power Mode)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>B15</td><td>B14</td><td>B13</td><td>B12</td><td>B11</td><td>B10</td><td>B9</td><td>B8</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0A</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>0</td><td>0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="19">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th></tr>
<tr><td>D7</td><td>Booster Voltage Status</td><td></td></tr>
<tr><td>D6</td><td>Idle Mode On/Off</td><td></td></tr>
<tr><td>D5</td><td>Partial Mode On/Off</td><td></td></tr>
<tr><td>D4</td><td>Sleep In/Out</td><td></td></tr>
<tr><td>D3</td><td>Display Normal Mode On/Off</td><td></td></tr>
<tr><td>D2</td><td>Display On/Off</td><td></td></tr>
<tr><td>D1</td><td>Not Defined</td><td>Set to ‘0’</td></tr>
<tr><td>D0</td><td>Not Defined</td><td>Set to ‘0’</td></tr>
</table>
• Bit D7 – Booster Voltage Status
‘0’ = Booster Off or has a fault.
‘1’ = Booster On and working OK (Meets optical characteristic. See chapter 8.7).
• Bit D6 - Idle Mode On/Off
‘0’ = Idle Mode Off.
‘1’ = Idle Mode On.
• Bit D5 – Partial Mode On/Off
‘0’ = Partial Mode Off.
‘1’ = Partial Mode On.
• Bit D4 – Sleep In/Out
‘0’ = Sleep In Mode.
‘1’ = Sleep Out Mode.
• Bit D3 – Display Normal Mode On/Off
‘0’ = Display Normal Mode Off.
‘1’ = Display Normal Mode On.
• Bit D2 – Display On/Off
‘0’ = Display is Off.
‘1’ = Display is On.
• Bit D1 – Not Defined
‘This bit is not applicable for this project, so it is set to ‘0’
• Bit D0 – Not Defined
‘This bit is not applicable for this project, so it is set to ‘0’

X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="19"></td></tr>
</table>

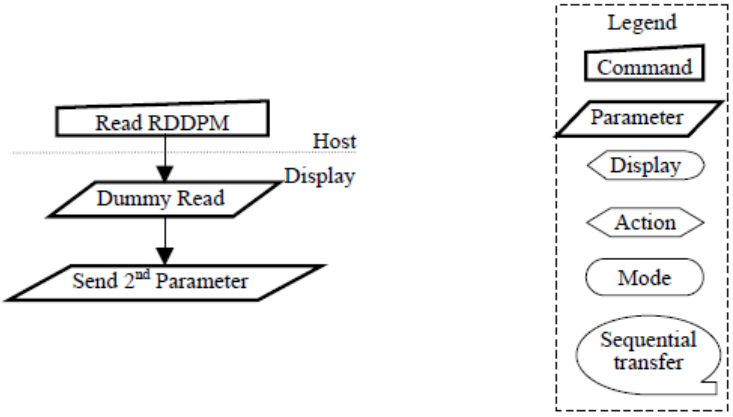
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

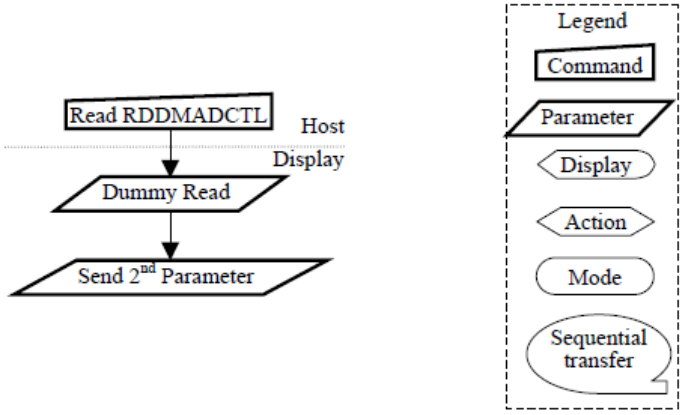
Status	Default Value
Power On Sequence	08_{HEX}
SW Reset	08_{HEX}
HW Reset	08_{HEX}

Flow Chart



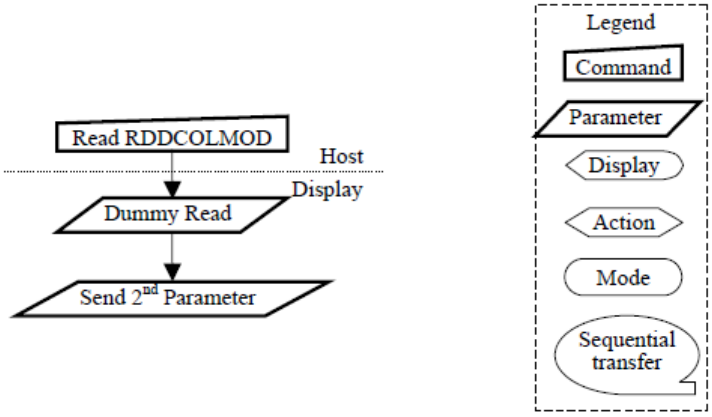
7.2.6. Read Display MADCTL (0Bh)

<table>
<tr><th>0B H</th><th colspan="19">RDDMADCTL (Read Display MADCTL)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>B15</td><td>B14</td><td>B13</td><td>B12</td><td>B11</td><td>B10</td><td>B9</td><td>B8</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0B</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>0</td><td>0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="19">
This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th></tr>
<tr><td>D7</td><td>Page Address Order</td><td></td></tr>
<tr><td>D6</td><td>Column Address Order</td><td></td></tr>
<tr><td>D5</td><td>Page/Column Order</td><td></td></tr>
<tr><td>D4</td><td>Line Address Order</td><td></td></tr>
<tr><td>D3</td><td>RGB/BGR Order</td><td></td></tr>
<tr><td>D2</td><td>Display Data Latch Order</td><td></td></tr>
<tr><td>D1</td><td>Switching between Segment outputs and RAM</td><td>Set to ‘0’</td></tr>
<tr><td>D0</td><td>Switching between Common outputs and RAM</td><td>Set to ‘0’</td></tr>
</table>
• Bit D7 – Page Address Order
‘0’ = Top to Bottom (When MADCTL B7=’0’).
‘1’ = Bottom to Top (When MADCTL B7=’1’).
• Bit D6 – Column Address Order
‘0’ = Left to Right (When MADCTL B6=’0’).
‘1’ = Right to Left (When MADCTL B6=’1’).
• Bit D5 - Page/Column Order
‘0’ = Normal Mode (When MADCTL B5=’0’).
‘1’ = Reverse Mode (When MADCTL B5=’1’).
Note: For Bits D7 to D5, also refer to Section 8.2.3 MCU to memory write/read direction.
• Bit D4 – Line Address Order
‘0’ = LCD Refresh Top to Bottom (When MADCTL B4=’0’).
‘1’ = LCD Refresh Bottom to Top (When MADCTL B4=’1’).
• Bit D3 – RGB/BGR Order
‘0’ = RGB (When MADCTL B3=’0’).
‘1’ = BGR (When MADCTL B3=’1’).
• Bit D2 – Display Data Latch Data Order
‘0’ = LCD Refresh Left to Right (When MADCTL B2=’0’).
‘1’ = LCD Refresh Right to Left (When MADCTL B2=’1’).
Note: For Bits D4, D3 and D2 also refer to 9.2.29 Memory Access Control (36h).
• Bit D1 – Switching Between Segment Outputs and RAM
This bit is not applicable for this project, so it is set to ‘0’
• Bit D0 – Switching Between Common Outputs and RAM
This bit is not applicable for this project, so it is set to ‘0’
X = Don’t care
</td></tr>
</table>

<table>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00_{HEX}</td></tr>
<tr><td>SW Reset</td><td>No Change</td></tr>
<tr><td>HW Reset</td><td>00_{HEX}</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

7.2.7. Read Display Pixel Format (0Ch)

<table>
<tr><td>0C H</td><td colspan="19">RDDCOLMOD (Read Display COLMOD)</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>B15</td><td>B14</td><td>B13</td><td>B12</td><td>B11</td><td>B10</td><td>B9</td><td>B8</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0C</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>D2</td><td>D1</td><td>D0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="19">
This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th></tr>
<tr><td>D7</td><td rowspan="4">RGB Interface Colour Format</td><td>Set to ‘0’</td></tr>
<tr><td>D6</td><td>Set to ‘0’</td></tr>
<tr><td>D5</td><td>Set to ‘0’</td></tr>
<tr><td>D4</td><td>Set to ‘0’</td></tr>
<tr><td>D3</td><td rowspan="4">Control Interface Colour Format</td><td>Set to ‘0’</td></tr>
<tr><td>D2</td><td></td></tr>
<tr><td>D1</td><td></td></tr>
<tr><td>D0</td><td></td></tr>
</table>
• Bit D7 – RGB Interface Colour Format Selection
This bit is not applicable for this project, so it is set to ‘0’.
• Bits D6, D5, D4 – RGB Interface Colour Pixel Format Definition
These bits are not applicable for this project, so they are set to ‘0’s.
• Bit D3 – Control Interface Colour Format Selection
This bit is not applicable for this project, so it is set to ‘0’.
• Bit D2, D1, D0 – Control Interface Colour Format Selection
See section “9.2.33. Interface Pixel Format (3Ah)”.
<table>
<tr><th>Control Interface Colour Format</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>Not Defined</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Not defined</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Not defined</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>12 bit/pixel</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Not Defined</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>16 bit/pixel</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>18 bit/pixel</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>24 bit/pixel</td><td>1</td><td>1</td><td>1</td></tr>
</table>
X = Don’t care
</td></tr>
<tr><td>Restriction</td><td colspan="19"></td></tr>
</table>

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>24 bit/pixel</td></tr>
<tr><td>SW Reset</td><td>No Change</td></tr>
<tr><td>HW Reset</td><td>24 bit/pixel</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>


</td></tr>
</table>

7.2.8. Read Display Image Mode (0Dh)

0D H	RDDIM (Read Display Image Mode)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	0	0	1	1	0	1	0D
1st parameter	1	↑	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
2nd parameter	1	↑	1	X	X	X	X	X	X	X	X	D7	0	D5	0	0	D2	D1	D0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Vertical Scrolling On/Off	
D6	Horizontal Scrolling Status	Set to '0'
D5	Inversion On/Off	
D4	All Pixels On	Set to '0'
D3	All Pixels Off	Set to '0'
D2	Gamma Curve Selection	
D1		
D0		

- Bit D7 – Vertical Scrolling On/Off
  '0' = Vertical Scrolling is Off.
  '1' = Vertical Scrolling is On.
- Bit D6 – Horizontal Scrolling Status
  This bit is not applicable for this project, so it is set to '0'
- Bit D5 – Inversion On/Off
  '0' = Inversion is Off.
  '1' = Inversion is On.
- Bit D4 – All Pixels On
  This bit is not applicable for this project, so it is set to '0'
- Bit D3 – All Pixels Off
  This bit is not applicable for this project, so it is set to '0'
- Bits D2, D1, D0 – Gamma Curve Selection

Gamma Curve Selection	D2	D1	D0	Gamma Set (26h) Parameter
Gamma Curve 1	0	0	0	GC0
Gamma Curve 2	0	0	1	GC1
Gamma Curve 3	0	1	0	GC2
Gamma Curve 4	0	1	1	GC3
Not Defined	1	0	0	Not Defined
Not Defined	1	0	1	Not Defined
Not Defined	1	1	0	Not Defined
Not Defined	1	1	1	Not Defined

X = Don't care

Restriction

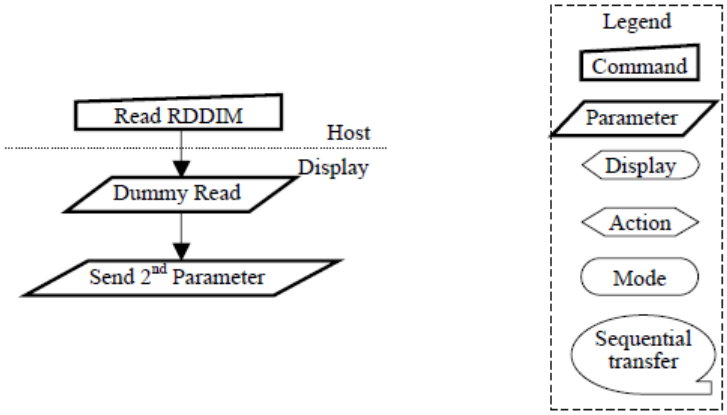
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00_{HEX}
SW Reset	00_{HEX}
HW Reset	00_{HEX}

Flow Chart



7.2.9. Read Display Signal Mode (0Eh)

0E H	RDDSM (Read Display Signal Mode)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	0	0	1	1	1	0	0E
1st parameter	1	↑	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
2nd parameter	1	↑	1	X	X	X	X	X	X	X	X	D7	D6	0	0	0	0	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Tearing Effect Line On/Off	
D6	Tearing Effect Line Output Mode	
D5	Horizontal Sync. (RGB I/F) On/Off	Set to '0'
D4	Vertical Sync. (RGB I/F) On/Off	Set to '0'
D3	Pixel Clock (PCLK, RGB I/F) On/Off	Set to '0'
D2	Data Enable (DE, RGB I/F)) On/Off	Set to '0'
D1	-	Set to '0'
D0	-	Set to '0'

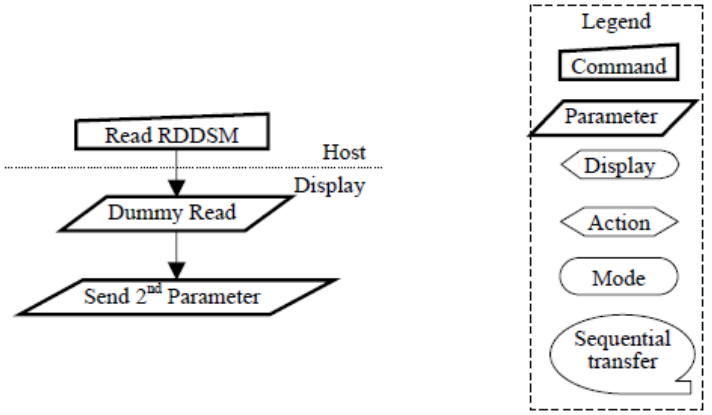
- Bit D7 – Tearing Effect Line On/Off
  '0' = Tearing Effect Line Off.
  '1' = Tearing Effect On.
- Bit D6 – Tearing Effect Line Output Mode, see section 8.3 for mode definitions.
  '0' = Mode 1.
  '1' = Mode 2.
- Bit D5 – Horizontal Sync. (RGB I/F) On/Off
  This bit is not applicable for this project, so it is set to '0'
- Bit D4 – Vertical Sync. (RGB I/F) On/Off
  This bit is not applicable for this project, so it is set to '0'
- Bit D3 – Pixel Clock (PCLK, RGB I/F) On/Off
  This bit is not applicable for this project, so it is set to '0'
- Bit D2 – Data Enable (DE, RGB I/F)) On/Off
  This bit is not applicable for this project, so it is set to '0'
- Bits D1, D0 - are for future use and are set to '0'.

X = Don't care

Restriction

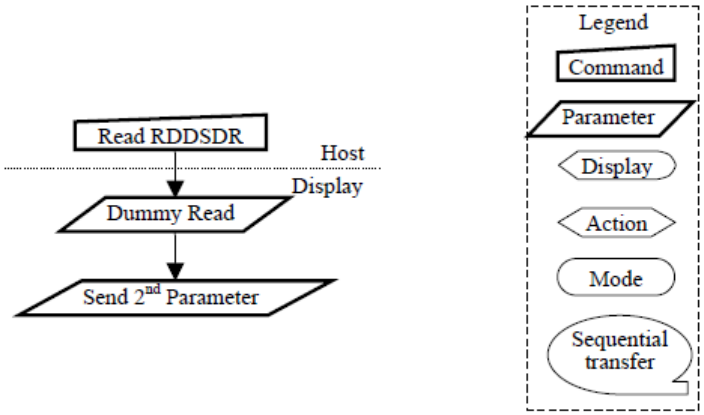
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

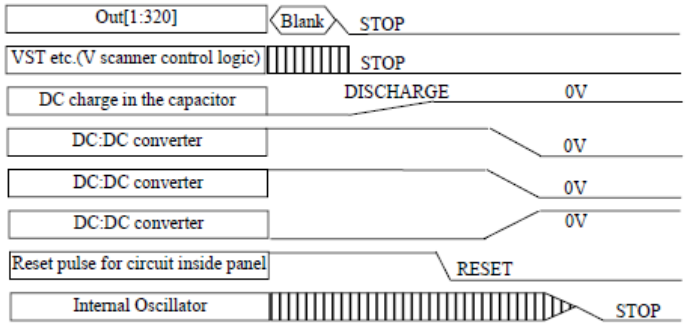
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00_{HEX}</td></tr><tr><td>SW Reset</td><td>00_{HEX}</td></tr><tr><td>HW Reset</td><td>00_{HEX}</td></tr></table>
Flow Chart	

7.2.10. Read Display Self-Diagnostic Result (0Fh)

<table>
<tr><th>0F H</th><th colspan="19">RDDSDR (Read Display Self Diagnostic Result)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>B15</td><td>B14</td><td>B13</td><td>B12</td><td>B11</td><td>B10</td><td>B9</td><td>B8</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0F</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>0</td><td>0</td><td>0</td><td>0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="19">This command indicates the status of the display self-diagnostic results after Sleep Out –command as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th></tr>
<tr><td>D7</td><td>Register Loading Detection</td><td></td></tr>
<tr><td>D6</td><td>Functionality Detection</td><td></td></tr>
<tr><td>D5</td><td>Chip Attachment Detection</td><td>Set to ‘0’</td></tr>
<tr><td>D4</td><td>Display Glass Break Detection</td><td>Set to ‘0’</td></tr>
<tr><td>D3</td><td>-</td><td>Set to ‘0’</td></tr>
<tr><td>D2</td><td>-</td><td>Set to ‘0’</td></tr>
<tr><td>D1</td><td>-</td><td>Set to ‘0’</td></tr>
<tr><td>D0</td><td>-</td><td>Set to ‘0’</td></tr>
</table>
• Bit D7 – Register Loading Detection
See section 8.10.1.
• Bit D6 – Functionality Detection
See section 8.10.2.
• Bit D5 – Chip Attachment Detection
This function is not implemented, so it is set to ‘0’.
• Bit D4 – Display Glass Break Detection
This function is not implemented, so it is set to ‘0’.
• Bits D3, D2, D1 and D0 are for future use and are set to ‘0’.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="19"></td></tr>
<tr><td>Register Availability</td><td colspan="19">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="19">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00HEX</td></tr>
<tr><td>SW Reset</td><td>00HEX</td></tr>
<tr><td>HW Reset</td><td>00HEX</td></tr>
</table>
</td></tr>
</table>

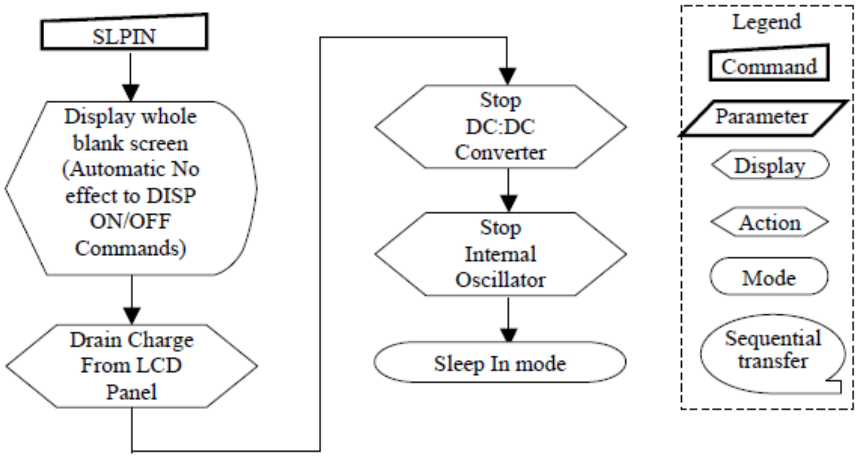
Flow Chart	 Read RDDSDR Host Display Dummy Read Send 2nd Parameter Legend Command Parameter Display Action Mode Sequential transfer

7.2.11. Sleep In (10h)

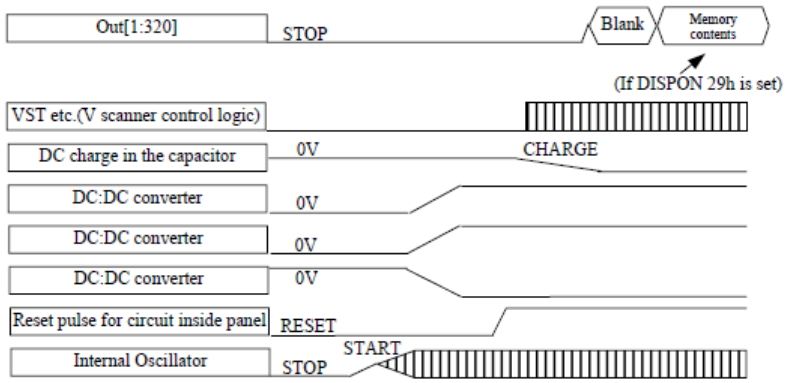
10 H	SLPIN (Sleep In)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	0	1	0	0	0	0	10
Parameter	NO PARAMETER																			
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.  MCU interface and memory are still working and the memory keeps its contents. See also section 8.6.2. X = Don't care																		
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilise. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.																		
Register Availability																			
Default																			

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

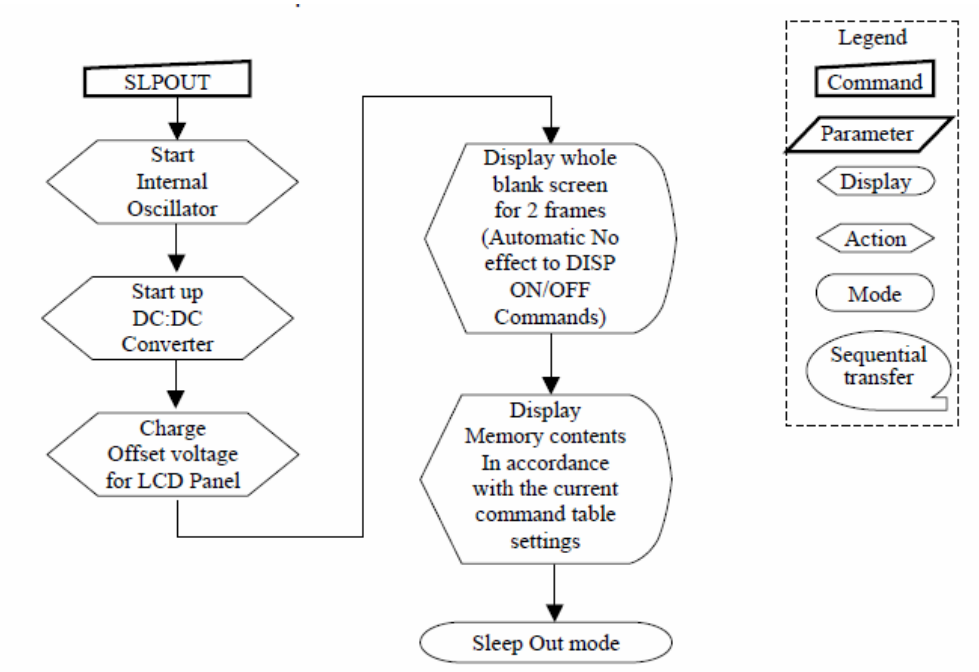
Status	Default Value
Power On Sequence	Sleep In Mode
SW Reset	Sleep In Mode
HW Reset	Sleep In Mode

Flow Chart	It takes 120msec to get into Sleep In mode after SLPIN command issued. 

7.2.12. Sleep Out (11h)

11 H	SLPOUT (Sleep Out)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	0	1	0	0	0	1	11
Parameter	NO PARAMETER																			
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.  See also section 8.6.2. X = Don't care																			
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilise. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. See also section 0. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.																			
Register Availability																			

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

<table>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr>
<tr><td>SW Reset</td><td>Sleep In Mode</td></tr>
<tr><td>HW Reset</td><td>Sleep In Mode</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>It takes 120msec to become Sleep Out mode after SLPOUT command issued.
 
</td></tr>
</table>

7.2.13. Partial Mode On (12h)

12 H	PTLON (Partial Mode On)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	0	1	0	0	1	0	12
Parameter	NO PARAMETER																			
Description	This command turns on partial mode. The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written. See also section 8.6.2. X = Don't care																		
Restriction	This command has no effect when Partial mode is active.																		
Register Availability																			
Default																			
Flow Chart	See Partial Area (30h)																		

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

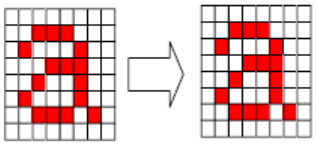
Status	Default Value
Power On Sequence	Normal Display Mode On
SW Reset	Normal Display Mode On
HW Reset	Normal Display Mode On

7.2.14. Normal Display Mode On (13h)

<table>
<tr><th>13 H</th><th colspan="19">NORON (Normal Display Mode On)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>B15</td><td>B14</td><td>B13</td><td>B12</td><td>B11</td><td>B10</td><td>B9</td><td>B8</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13</td></tr>
<tr><td>Parameter</td><td colspan="20">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="20">This command returns the display to normal mode.
Normal display mode on means Partial mode off, Scroll mode Off.
See also section 8.6.2.

X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="20">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="20"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="20"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode On</td></tr><tr><td>SW Reset</td><td>Normal Display Mode On</td></tr><tr><td>HW Reset</td><td>Normal Display Mode On</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="20">See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command.</td></tr>
</table>

7.2.15. Display Inversion Off (20h)

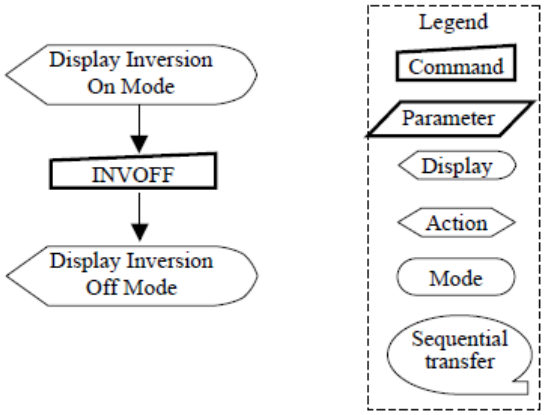
20 H	INVOFF (Display Inversion Off)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	1	0	0	0	0	0	20
Parameter	NO PARAMETER																			
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. (Example) memory display  X = don't care																		
Restriction	This command has no effect when module is already in inversion off mode.																		

Register Availability

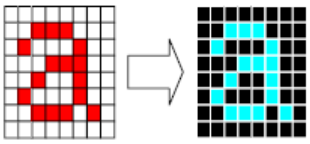
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion Off
SW Reset	Display Inversion Off
HW Reset	Display Inversion Off

Flow Chart	 Display Inversion On Mode INVOFF Display Inversion Off Mode Legend Command Parameter Display Action Mode Sequential transfer

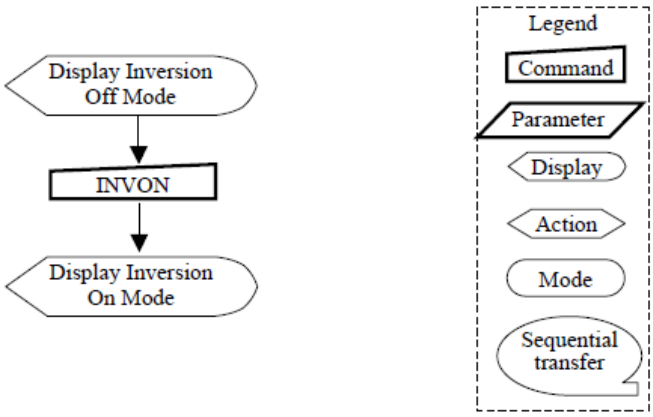
7.2.16. Display Inversion On (21h)

21 H	INVON (Display Inversion On)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	1	0	0	0	0	1	21
Parameter	NO PARAMETER																			
Description	This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status. (Example) memory display  X = don't care																		
Restriction	This command has no effect when module is already in inversion on mode.																		
Register Availability																			

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

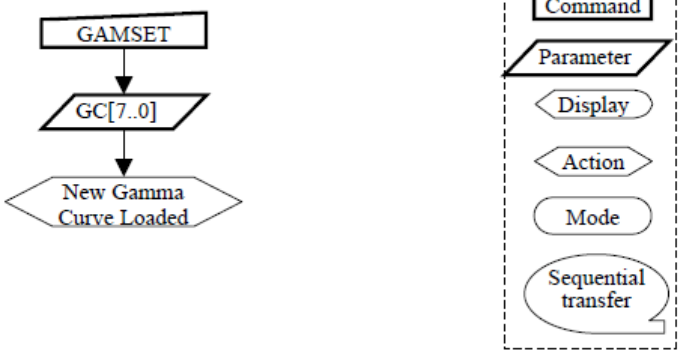
Status	Default Value
Power On Sequence	Display Inversion Off
SW Reset	Display Inversion Off
HW Reset	Display Inversion Off

Flow Chart	

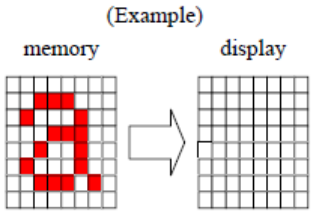
Display Inversion Off Mode
INVON
Display Inversion On Mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

7.2.17. Gamma Set (26h)

<table>
<tr><th>26 H</th><th colspan="20">GAMSET (Gamma Set)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>B15</td><td>B14</td><td>B13</td><td>B12</td><td>B11</td><td>B10</td><td>B9</td><td>B8</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>26</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>GC7</td><td>GC6</td><td>GC5</td><td>GC4</td><td>GC3</td><td>GC2</td><td>GC1</td><td>GC0</td><td>1..08</td></tr>
<tr><td>Description</td><td colspan="20">This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curves are defined in Section “8.7 Gamma Curve”.
The curve is selected by setting the appropriate bit in the parameter as described in the Table:
<table><tr><th>GC[7…0]</th><th>Parameter</th><th>Curve Selected</th></tr><tr><td>01h</td><td>GC0</td><td>Gamma Curve 1</td></tr><tr><td>02h</td><td>GC1</td><td>Gamma Curve 2</td></tr><tr><td>04h</td><td>GC2</td><td>Gamma Curve 3</td></tr><tr><td>08h</td><td>GC3</td><td>Gamma Curve 4</td></tr></table>Note: All other values are undefined.
X = don’t care</td></tr>
<tr><td>Restriction</td><td colspan="20">Values of GC[7..0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.</td></tr>
<tr><td>Register Availability</td><td colspan="20"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="20"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>01_{HEX}</td></tr><tr><td>SW Reset</td><td>01_{HEX}</td></tr><tr><td>HW Reset</td><td>01_{HEX}</td></tr></table></td></tr>
</table>

Flow Chart	 GAMSET GC[7..0] New Gamma Curve Loaded Legend Command Parameter Display Action Mode Sequential transfer

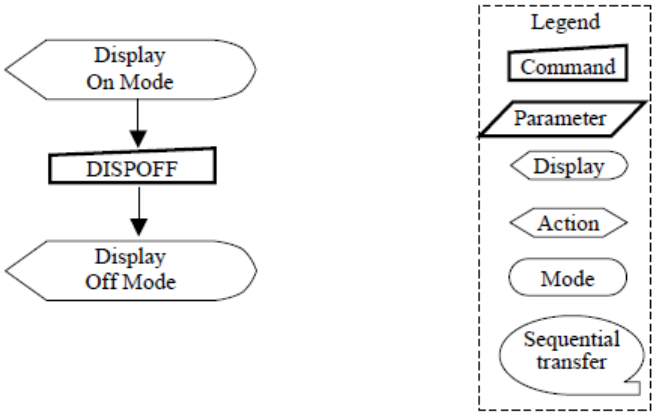
7.2.18. Display Off (28h)

28 H	DISPOFF (Display Off)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	1	0	1	0	0	0	28
Parameter	NO PARAMETER																			
Description	In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display.  X = don't care.																		
Restriction	This command has no effect when module is already in display off mode.																		
Register Availability																			

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

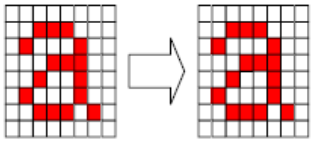
Default

Status	Default Value
Power On Sequence	Display Off
SW Reset	Display Off
HW Reset	Display Off

Flow Chart	

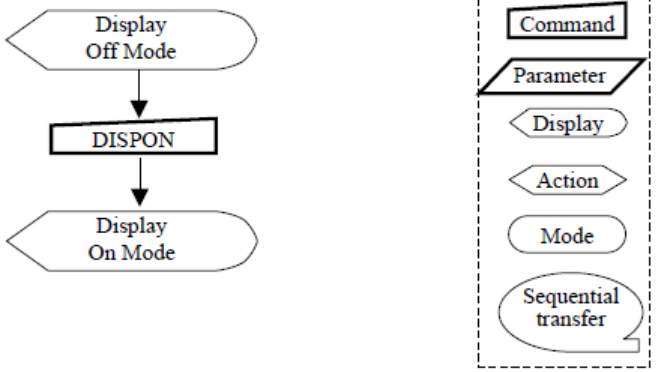
Display
On Mode
DISPOFF
Display
Off Mode
Legend
Command
Parameter
Display
Action
Mode
Sequential
transfer

7.2.19. Display On (29h)

29 H	DISPON (Display On)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	1	0	1	0	0	1	29
Parameter	NO PARAMETER																			
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example) memory display  X = don't care.																		
Restriction	This command has no effect when module is already in display on mode.																		
Register Availability																			
Default																			

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	Display Off
SW Reset	Display Off
HW Reset	Display Off

Flow Chart	

Display
Off Mode
DISPON
Display
On Mode
Legend
Command
Parameter
Display
Action
Mode
Sequential
transfer

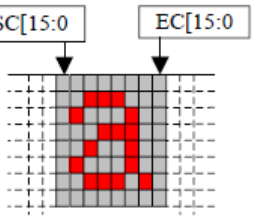
7.2.20. Column Address Set (2Ah)

2A H	CASET (Column Address Set)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	1	0	1	0	1	0	2A
1st parameter	1	1	↑	X	X	X	X	X	X	X	X	SC 15	SC 14	SC 13	SC 12	SC 11	SC 10	SC 9	SC 8	Note 1
2nd parameter	1	1	↑	X	X	X	X	X	X	X	X	SC 7	SC 6	SC 5	SC 4	SC 3	SC 2	SC 1	SC 0	
3rd parameter	1	1	↑	X	X	X	X	X	X	X	X	EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC 9	EC 8	Note 1
4th parameter	1	1	↑	X	X	X	X	X	X	X	X	EC 7	EC 6	EC 5	EC 4	EC 3	EC 2	EC 1	EC 0	

Description

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.

(Example)



X = don't care

Restriction

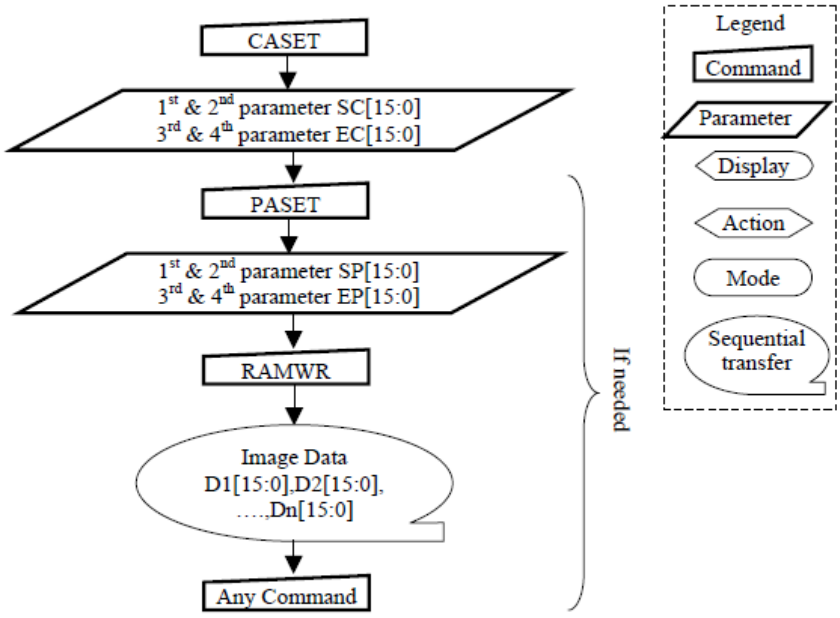
SC[15:0] always must be equal to or less than EC[15:0].
Note 1: When SC[15:0] or EC[15:0] is greater than 00EFh (When MADCTL's B5 = 0) or 013Fh (When MADCTL's B5 = 1), data of out of range will be ignored

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	$SC[15:0]=0000_{HEX}$	$EC[15:0]=00EF_{HEX}$
SW Reset	$SC[15:0]=0000_{HEX}$	If MADCTL's B5 = 0: $EC[15:0]=00EF_{HEX}$
		If MADCTL's B5 = 1: $EC[15:0]=013F_{HEX}$
HW Reset	$SC[15:0]=0000_{HEX}$	$EC[15:0]=00EF_{HEX}$

Flow Chart	

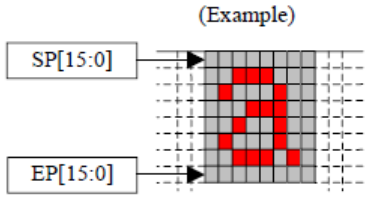
CASET
1st & 2nd parameter SC[15:0]
3rd & 4th parameter EC[15:0]
PASET
1st & 2nd parameter SP[15:0]
3rd & 4th parameter EP[15:0]
RAMWR
Image Data
D1[15:0],D2[15:0],
….,Dn[15:0]
Any Command
If needed
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

7.2.21. Page Address Set (2Bh)

2B H	PASET (Page Address Set)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	1	0	1	0	1	1	2B
1st parameter	1	1	↑	X	X	X	X	X	X	X	X	SP 15	SP 14	SP 13	SP 12	SP 11	SP 10	SP 9	SP 8	Note 1
2nd parameter	1	1	↑	X	X	X	X	X	X	X	X	SP 7	SP 6	SP 5	SP 4	SP 3	SP 2	SP 1	SP 0	
3rd parameter	1	1	↑	X	X	X	X	X	X	X	X	EP 15	EP 14	EP 13	EP 12	EP 11	EP 10	EP 9	EP 8	Note 1
4th parameter	1	1	↑	X	X	X	X	X	X	X	X	EP 7	EP 6	EP 5	EP 4	EP 3	EP 2	EP 1	EP 0	

Description

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes.
Each value represents one Page line in the Frame Memory.



X = don't care

Restriction

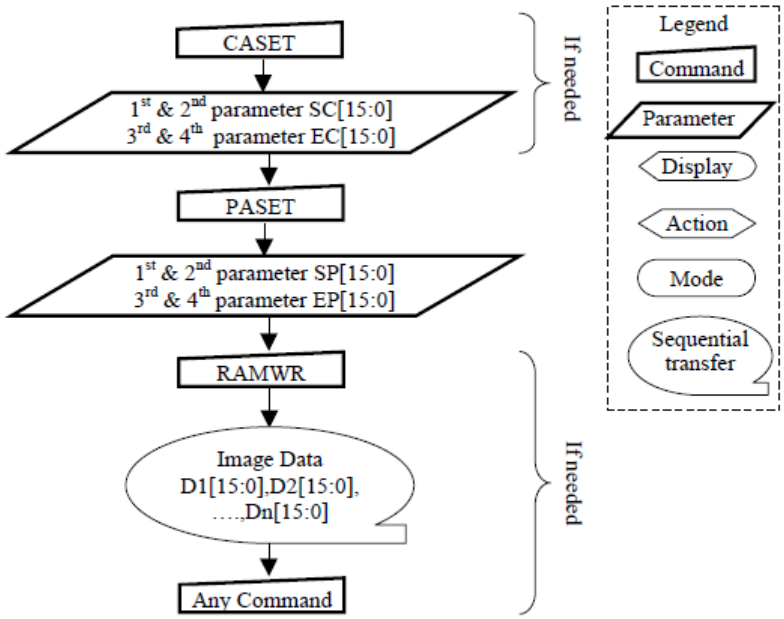
SP[15:0] always must be equal to or less than EP[15:0]
When SP[15:0] or EP[15:0] is greater than 013Fh (When MADCTL's B5 = 0) or 00EFh (When MADCTL's B5 = 1), data of out of range will be ignored.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SP[15:0]=0000_{HEX}	EP[15:0]=$013F_{HEX}$
SW Reset	SP[15:0]=0000_{HEX}	If MADCTL's B5 = 0: EP[15:0]=$013F_{HEX}$
		If MADCTL's B5 = 1: EP[15:0]=$00EF_{HEX}$
HW Reset	SP[15:0]=0000_{HEX}	EP[15:0]=$013F_{HEX}$

Flow Chart	

CASET
1st & 2nd parameter SC[15:0]
3rd & 4th parameter EC[15:0]
PASET
1st & 2nd parameter SP[15:0]
3rd & 4th parameter EP[15:0]
RAMWR
Image Data
D1[15:0],D2[15:0],
….,Dn[15:0]
Any Command
If needed
If needed
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

7.2.22. Memory Write (2Ch)

2C H	RAMWR (Memory Write)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	1	0	1	1	0	0	2C
1st parameter	1	1	↑	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000 … FFFF
:	1	1	↑	Dx 15	Dx 14	Dx 13	Dx 12	Dx 11	Dx 10	Dx 9	Dx 8	Dx 7	Dx 6	Dx 5	Dx 4	Dx 3	Dx 2	Dx 1	Dx 0	0000 … FFFF
NTH parameter	1	1	↑	Dn 15	Dn 14	Dn 13	Dn 12	Dn 11	Dn 10	Dn 9	Dn 8	Dn 7	Dn 6	Dn 5	Dn 4	Dn 3	Dn 2	Dn 1	Dn 0	0000 … FFFF

Description

This command is used to transfer data from MCU to frame memory.
This command makes no change to the other driver status.
When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.
The Start Column/Start Page positions are different in accordance with MADCTL setting. (See 8.2.3)
Then D[15:0] is stored in frame memory and the column register and the page register incremented as in Table 8.2.3.
Sending any other command can stop frame Write.
See section 8.1.5 “Display Module Data Colour Coding” for colour coding, when there is used 8 (16/8x is low - D[7:0] are used and D[15:8] are not used) or 16 (16/8X is high - D[15:0] are used) data lines for image data.

X = don’t care.

Restriction

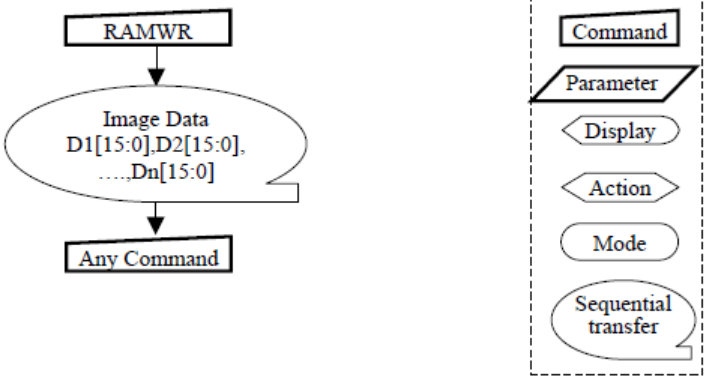
In all colour modes, there is no restriction on length of parameters.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart	 RAMWR Image Data D1[15:0],D2[15:0], …..,Dn[15:0] Any Command Legend Command Parameter Display Action Mode Sequential transfer

7.2.23. Colour Set (2Dh)

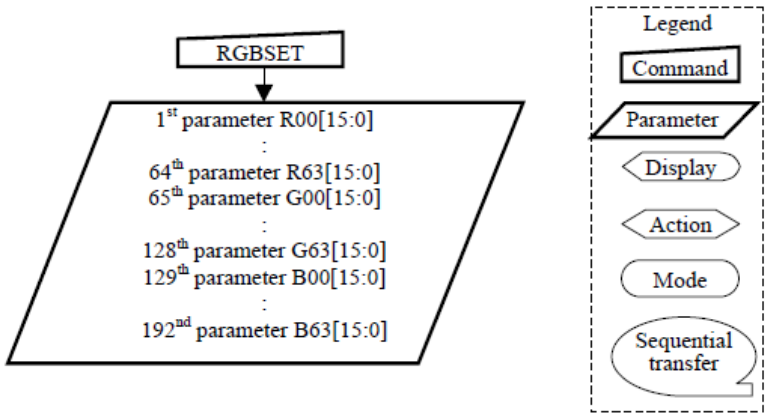
2D H	RGBSET (Colour Set)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	1	0	1	1	0	1	2D
1st parameter	1	1	↑	X	X	X	X	X	X	X	X	R007	R006	R005	R004	R003	R002	R001	R000	0000 … FFFF
:	1	1	↑	X	X	X	X	X	X	X	X	Rnn7	Rnn6	Rnn5	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	0000 … FFFF
64th parameter	1	1	↑	X	X	X	X	X	X	X	X	R637	R636	R635	R634	R633	R632	R631	R630	0000 … FFFF
65th parameter	1	1	↑	X	X	X	X	X	X	X	X	G007	G006	G005	G004	G003	G002	G001	G000	0000 … FFFF
:	1	1	↑	X	X	X	X	X	X	X	X	Gnn7	Gnn6	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	0000 … FFFF
128th parameter	1	1	↑	X	X	X	X	X	X	X	X	G637	G636	G635	G634	G633	G632	G631	G630	0000 … FFFF
129th parameter	1	1	↑	X	X	X	X	X	X	X	X	B007	B006	B005	B004	B003	B002	B001	B000	0000 … FFFF
:	1	1	↑	X	X	X	X	X	X	X	X	Bnn7	Bnn6	Bnn5	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	0000 … FFFF
192nd parameter	1	1	↑	X	X	X	X	X	X	X	X	B637	B636	B635	B634	B633	B632	B631	B630	0000 … FFFF
Description	This command is used to define the LUT for 12bit-to-24bit/16bit-to-24bit/18bit-to-24bit colour depth conversions. (See also section 8.9) 192 bytes must be written to the LUT regardless of the colour mode. Only the values in Section 8.9 are referred. This command has no effect on other commands/parameters and Contents of frame memory. Visible change takes effect next time the Frame Memory is written to. X = don't care.																		
Restriction																			
Register Availability																			

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Random values
SW Reset	Contents of LUT protected
HW Reset	Random values

Flow Chart



7.2.24. Memory Read (2Eh)

2E H	RAMRD (Memory Read)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	1	0	1	1	1	0	2E
1st parameter	1	↑	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	XXXX
2nd parameter	1	↑	1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0000 … FFFF
:	1	↑	1	Dx 15	Dx 14	Dx 13	Dx 12	Dx 11	Dx 10	Dx 9	Dx 8	Dx 7	Dx 6	Dx 5	Dx 4	Dx 3	Dx 2	Dx 1	Dx 0	0000 … FFFF
(N+1)TH parameter	1	↑	1	Dn 15	Dn 14	Dn 13	Dn 12	Dn 11	Dn 10	Dn 9	Dn 8	Dn 7	Dn 6	Dn 5	Dn 4	Dn 3	Dn 2	Dn 1	Dn 0	0000 … FFFF

Description

This command is used to transfer data from frame memory to MCU. See section 9.1.
This command makes no change to the other driver status.
When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.
The Start Column/Start Page positions are different in accordance with MADCTL setting. (See 8.2.3)
Then D[15:0] is read back from the frame memory and the column register and the page register incremented as in Table 8.2.3.
Frame Read can be stopped by sending any other command.
See section 8.1.5 “Display Module Data Colour Coding” for colour coding (24 bit cases), when there is used 8 or 16 data lines for image data.

X = don’t care.

Restriction

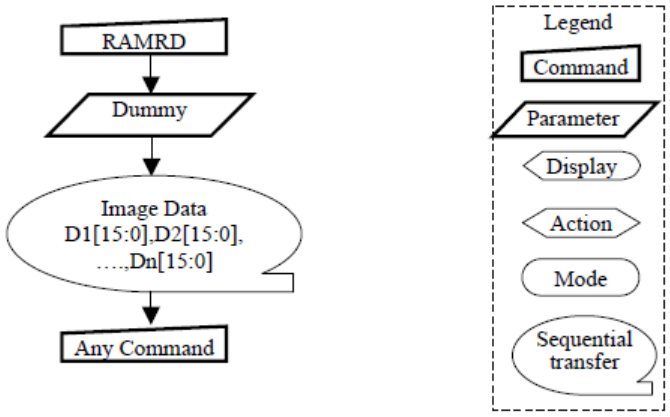
In all colour modes, the Frame Read is always 24 bit so there is no restriction on length of parameters.
Note – Memory Read is only possible via the Parallel Interface.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart	 RAMRD Dummy Image Data D1[15:0],D2[15:0], ….,Dn[15:0] Any Command Legend Command Parameter Display Action Mode Sequential transfer

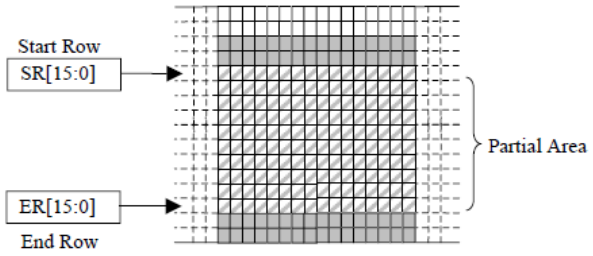
7.2.25. Partial Area (30h)

30 H	PLTAR (Partial Area)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	1	1	0	0	0	0	30
1st parameter	1	1	↑	X	X	X	X	X	X	X	X	SR 15	SR 14	SR 13	SR 12	SR 11	SR 10	SR 9	SR 8	0000 … 013F
2nd parameter	1	1	↑	X	X	X	X	X	X	X	X	SR 7	SR 6	SR 5	SR 4	SR 3	SR 2	SR 1	SR 0	
3rd parameter	1	1	↑	X	X	X	X	X	X	X	X	ER 15	ER 14	ER 13	ER 12	ER 11	ER 10	ER 9	ER 8	0000 … 013F
4th parameter	1	1	↑	X	X	X	X	X	X	X	X	ER 7	ER 6	ER 5	ER 4	ER 3	ER 2	ER 1	ER 0	

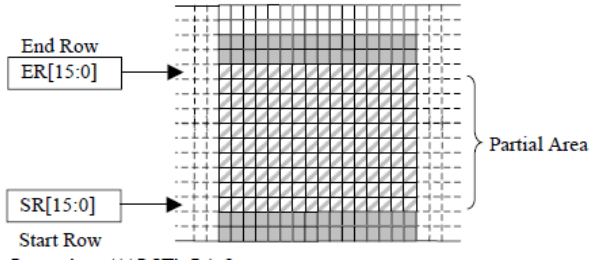
Description

This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.

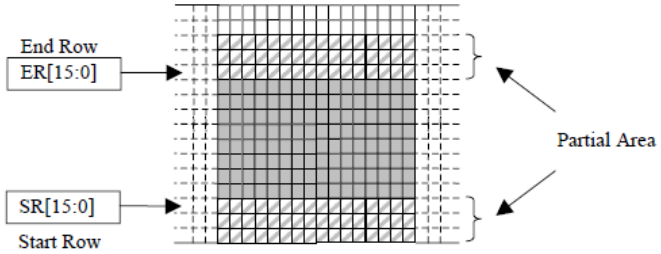
If End Row>Start Row when MADCTL B4=0:-



If End Row>Start Row when MADCTL B4=1:-



If End Row<Start Row when MADCTL B4=0:-



If End Row = Start Row then the Partial Area will be one row deep.

X = don't care.

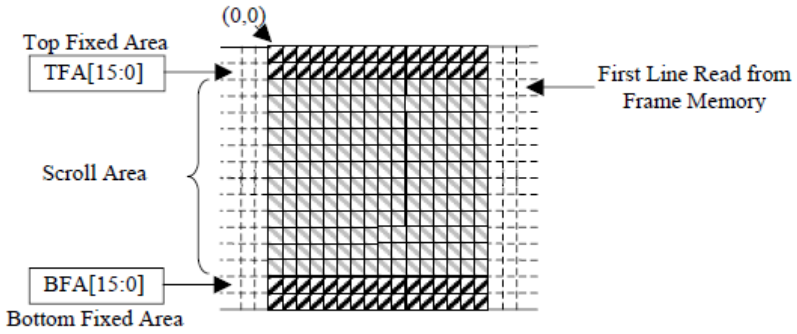
7.2.26. Vertical Scrolling Definition (33h)

33 H	VSCRDEF (Vertical Scrolling Definition)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	1	1	0	0	1	1	33
1st parameter	1	1	↑	X	X	X	X	X	X	X	X	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8	0000 … 0140
2nd parameter	1	1	↑	X	X	X	X	X	X	X	X	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0	
3rd parameter	1	1	↑	X	X	X	X	X	X	X	X	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8	0000 … 0140
4th parameter	1	1	↑	X	X	X	X	X	X	X	X	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0	
5th parameter	1	1	↑	X	X	X	X	X	X	X	X	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8	0000 … 0140
6th parameter	1	1	↑	X	X	X	X	X	X	X	X	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0	

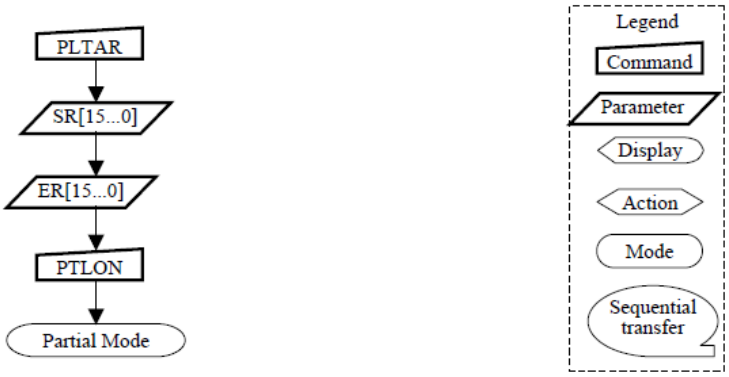
Description

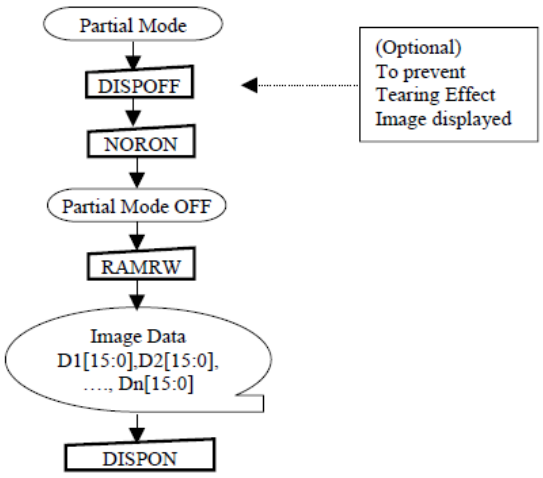
This command defines the Vertical Scrolling Area of the display.

When MADCTL B4=0
The 1st & 2nd parameter TFA[15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).
The 3rd & 4th parameter VSA[15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.
The 5th & 6th parameter BFA[15...0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
TFA, VSA and BFA refer to the Frame Memory Line Pointer.



X = don't care.

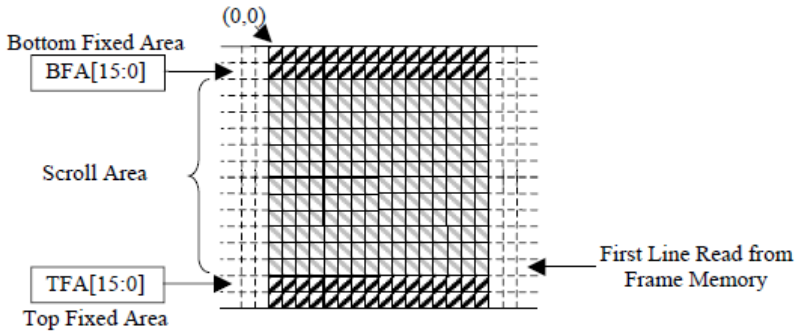
<table>
<tr><td>Restriction</td><td>SR[15…0] and ER[15…0] cannot be 0000h nor exceed 013Fh.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th colspan="2">Default Value</th></tr>
<tr><td>Power On Sequence</td><td>SR[15…0] = 0000_{HEX}</td><td>ER[15…0] = $013F_{HEX}$</td></tr>
<tr><td>SW Reset</td><td>SR[15…0] = 0000_{HEX}</td><td>ER[15…0] = $013F_{HEX}$</td></tr>
<tr><td>HW Reset</td><td>SR[15…0] = 0000_{HEX}</td><td>ER[15…0] = $013F_{HEX}$</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>
1. To Enter Partial Mode


2. To Leave Partial Mode


</td></tr>
</table>

Description

When MADCTL B4=1
The 1st & 2nd parameter TFA[15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
The 3rd & 4th parameter VSA[15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.
The 5th & 6th parameter BFA[15...0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



See also Section 8.2.2.2 for details of the Memory to Display mappings.

Restriction

The condition is TFA+VSA+BFA = 320, otherwise Scrolling mode is undefined.
In Vertical Scroll Mode, MADCTL B5 should be set to '0' – this only affects the Frame Memory Write.

Register Availability

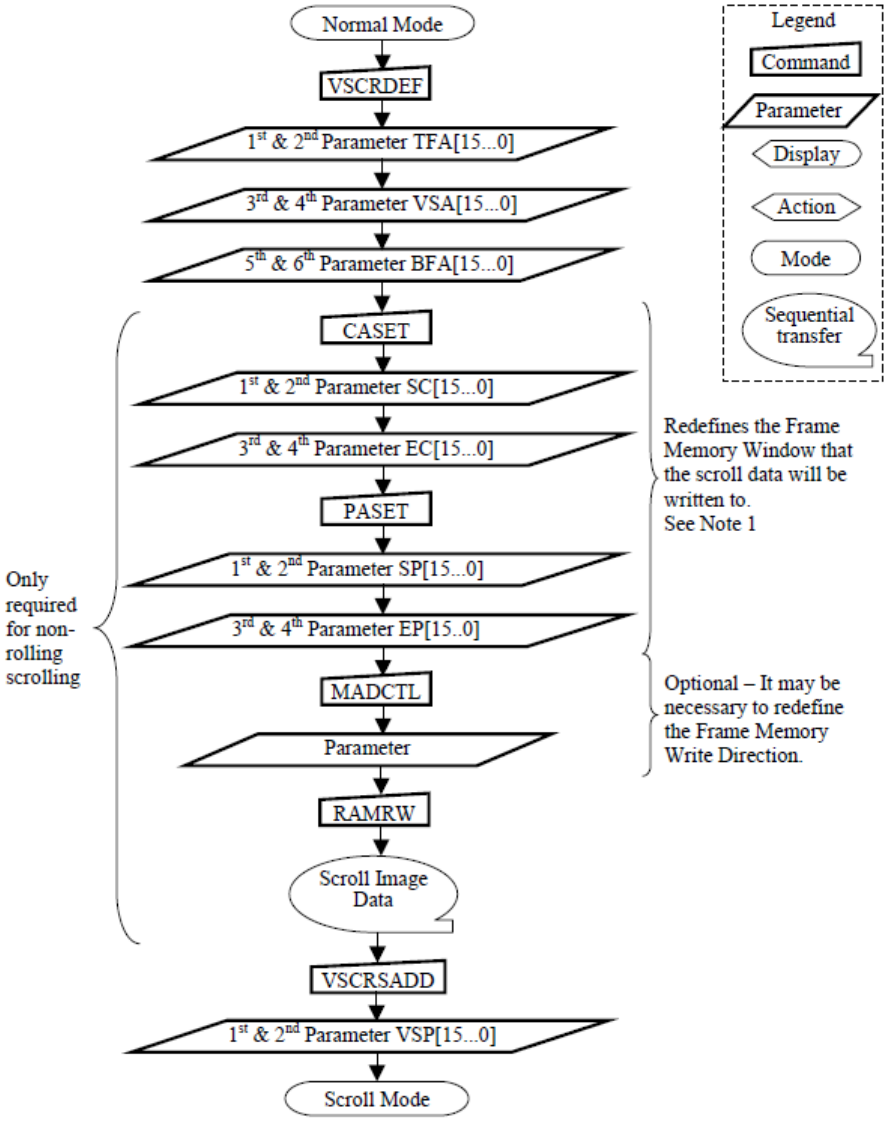
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
Power On Sequence	TFA[15…0] = 0000_{HEX}	VSA[15…0] = 0140_{HEX}	BFA[15…0] = 0000_{HEX}
SW Reset	TFA[15…0] = 0000_{HEX}	VSA[15…0] = 0140_{HEX}	BFA[15…0] = 0000_{HEX}
HW Reset	TFA[15…0] = 0000_{HEX}	VSA[15…0] = 0140_{HEX}	BFA[15…0] = 0000_{HEX}

Flow Chart

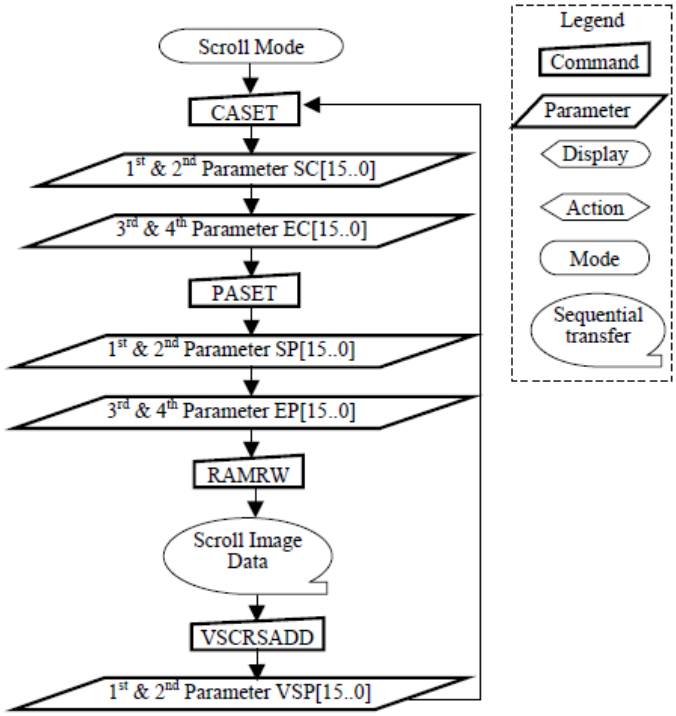
1. To enter Vertical Scroll Mode:



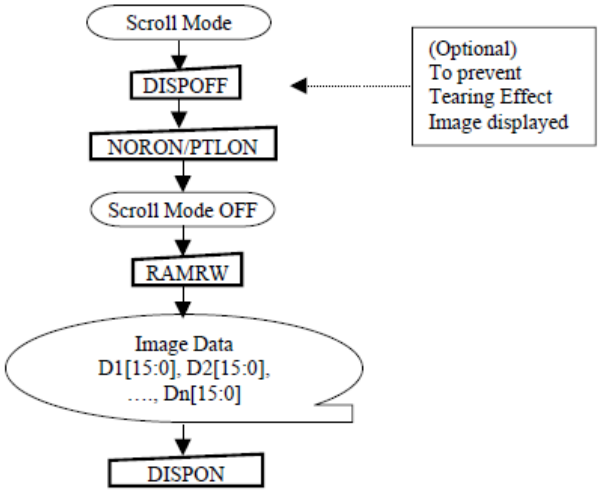
Note 1
The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

Flow Chart

2. Continuous Scroll:



3. To Leave Vertical Scroll Mode:



Note2: Scroll Mode can be left by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

7.2.27. Tearing Effect Line Off (34h)

34 H	TEOFF (Tearing Effect Line OFF)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	1	1	0	1	0	0	34
Parameter	NO PARAMETER																			
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line. X = don't care.																			
Restriction	This command has no effect when Tearing Effect output is already OFF.																			

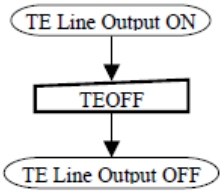
Register Availability

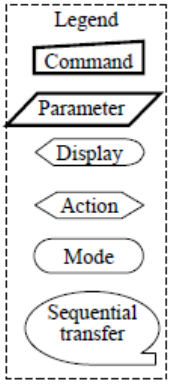
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
SW Reset	Off
HW Reset	Off

Flow Chart





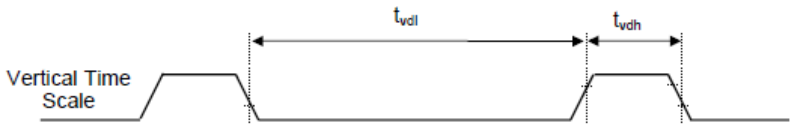
7.2.28. Tearing Effect Line On (35h)

35 H	TEON (Tearing Effect Line ON)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	1	1	0	1	0	1	35
Parameter	1	1	↑	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	M	XX

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4.
The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).

When M=0:
The Tearing Effect Output line consists of V-Blanking information only:



When M=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

X = don't care.

Restriction

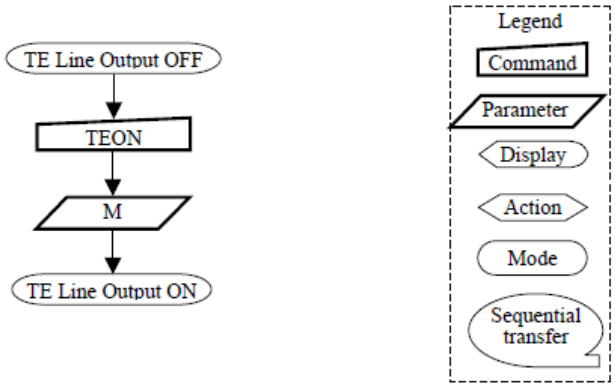
This command has no effect when Tearing Effect output is already ON.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
SW Reset	Off
HW Reset	Off

Flow Chart	 TE Line Output OFF TEON M TE Line Output ON Legend Command Parameter Display Action Mode Sequential transfer

7.2.29. Memory Access Control (36h)

36 H	MADCTL (Memory Access Control)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	1	1	0	1	1	0	36
Parameter	1	1	↑	X	X	X	X	X	X	X	X	D7	D6	D5	D4	D3	D2	X	X	XX

Description

This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.

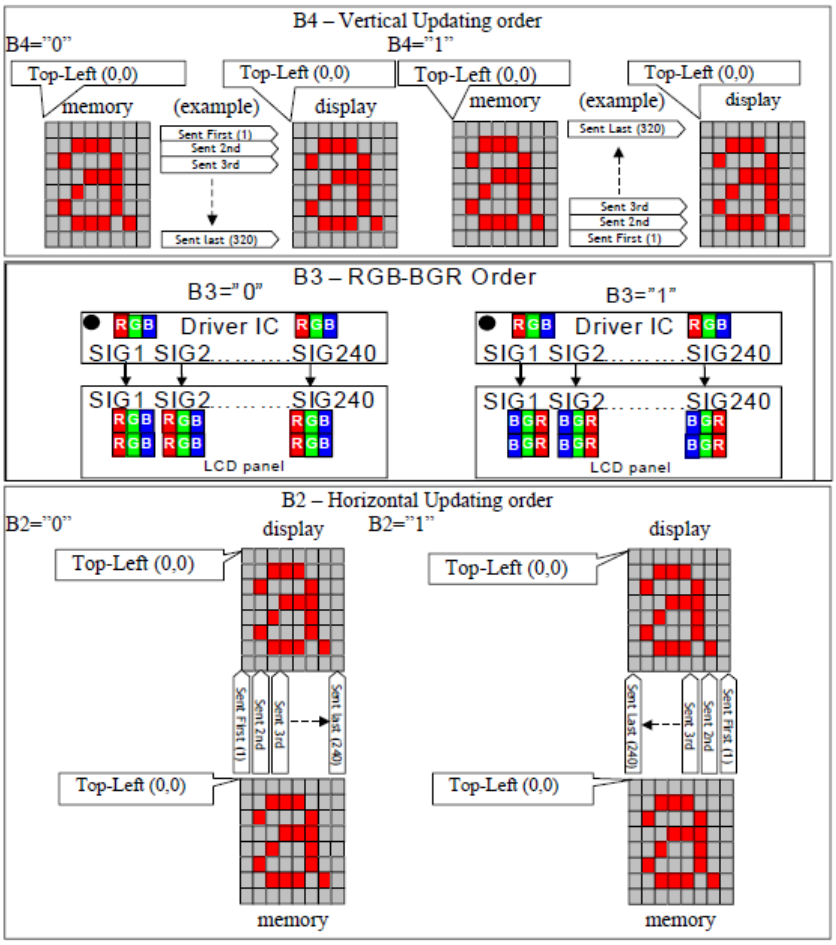
Bit	Description	Comment
D7	Page Address Order	
D6	Column Address Order	
D5	Page/Column Order	
D4	Line Address Order	
D3	RGB/BGR Order	
D2	Display Data Latch Order	
D1	Switching between Segment outputs and RAM	Don't care
D0	Switching between Common outputs and RAM	Don't care

- Bit D7 – Page Address Order
  '0' = Top to Bottom (When MADCTL B7='0').
  '1' = Bottom to Top (When MADCTL B7='1').
- Bit D6 – Column Address Order
  '0' = Left to Right (When MADCTL B6='0').
  '1' = Right to Left (When MADCTL B6='1').
- Bit D5 - Page/Column Order
  '0' = Normal Mode (When MADCTL B5='0').
  '1' = Reverse Mode (When MADCTL B5='1').

Note: For Bits D7 to D5, also refer to Section 8.2.3 MCU to memory write/read direction.

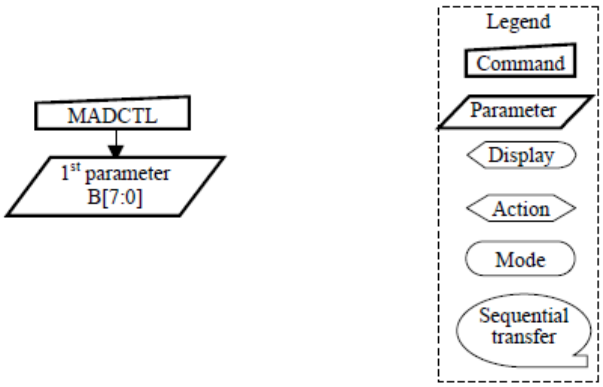
- Bit D4 – Line Address Order
  '0' = LCD Refresh Top to Bottom (When MADCTL B4='0').
  '1' = LCD Refresh Bottom to Top (When MADCTL B4='1').
- Bit D3 – RGB/BGR Order
  '0' = RGB (When MADCTL B3='0').
  '1' = BGR (When MADCTL B3='1').
- Bit D2 – Display Data Latch Data Order
  '0' = LCD Refresh Left to Right (When MADCTL B2='0').
  '1' = LCD Refresh Right to Left (When MADCTL B2='1').
- Bit D1 – Switching Between Segment Outputs and RAM
  This bit is not applicable for this project, so it is set to '0'
- Bit D0 – Switching Between Common Outputs and RAM
  This bit is not applicable for this project, so it is set to '0'

X = don't care.

Description	 Note: Top-Left (0,0) means a physical memory location.
Restriction	
Register Availability	
Default	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	0000 0000_{HEX}
SW Reset	No Change
HW Reset	0000 0000_{HEX}

Flow Chart	 MADCTL 1st parameter B[7:0] Legend Command Parameter Display Action Mode Sequential transfer

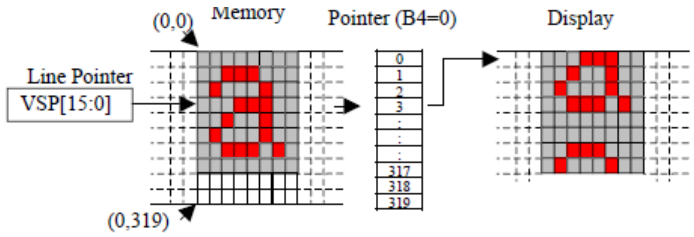
7.2.30. Vertical Scrolling Start Address (37h)

37 H	VSCRSADD (Vertical Scrolling Start Address)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	1	1	0	1	1	1	37
1st parameter	1	1	↑	X	X	X	X	X	X	X	X	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8	0000 … 013F
2nd parameter	1	1	↑	X	X	X	X	X	X	X	X	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0	

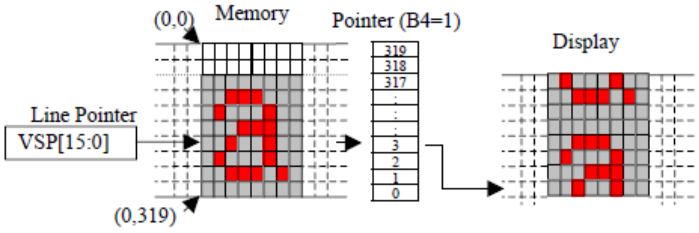
Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.
The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-

When MADCTL B4=0
Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.



When MADCTL B4=1
Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.



Notes:
When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.

VSP refers to the Frame Memory line Pointer.
X = don't care

Restriction

Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) – otherwise undesirable image will be displayed on the Panel.

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0000_{HEX}</td></tr>
<tr><td>SW Reset</td><td>0000_{HEX}</td></tr>
<tr><td>HW Reset</td><td>0000_{HEX}</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

7.2.31. Idle Mode Off (38h)

38 H	IDMOFF (Idle mode off)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	1	1	1	0	0	0	38
Parameter	NO PARAMETER																			
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 16,777,216 colours. See also section 8.6.2. X = don't care.																			
Restriction	This command has no effect when module is already in idle off mode.																			

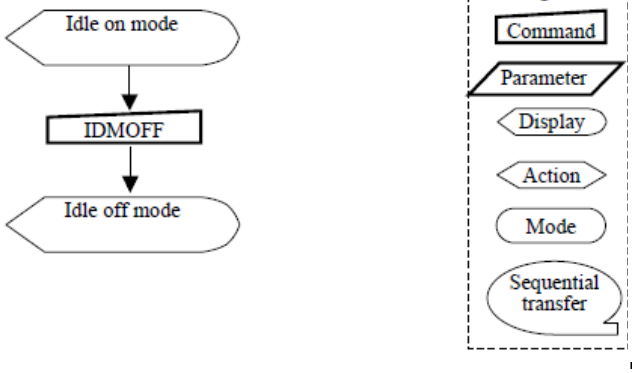
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
SW Reset	Idle Mode Off
HW Reset	Idle Mode Off

Flow Chart



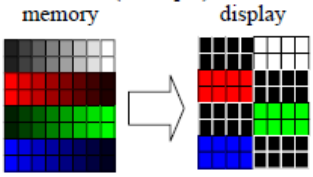
7.2.32. Idle Mode On (39h)

39 H	IDMON (Idle mode on)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	0	0	1	1	1	0	0	1	39
Parameter	NO PARAMETER																			

Description

This command is used to enter into Idle mode on.
In the idle on mode, colour expression is reduced. The primary and the secondary colours using MSB of each R, G and B in the Frame Memory, 8 colour depth data is displayed.

(Example)



Memory contents vs Display Colour			
	R7 R6 R5 R4 R3 R2 R1 R0	G7 G6 G5 G4 G3 G2 G1 G0	B7 B6 B5 B4 B3 B2 B1 B0
Black	0XXXXXXX	0XXXXXXX	0XXXXXXX
Blue	0XXXXXXX	0XXXXXXX	1XXXXXXX
Red	1XXXXXXX	0XXXXXXX	0XXXXXXX
Magenta	1XXXXXXX	0XXXXXXX	1XXXXXXX
Green	0XXXXXXX	1XXXXXXX	0XXXXXXX
Cyan	0XXXXXXX	1XXXXXXX	1XXXXXXX
Yellow	1XXXXXXX	1XXXXXXX	0XXXXXXX
White	1XXXXXXX	1XXXXXXX	1XXXXXXX

See also section 8.6.2.

X = don't care.

Restriction

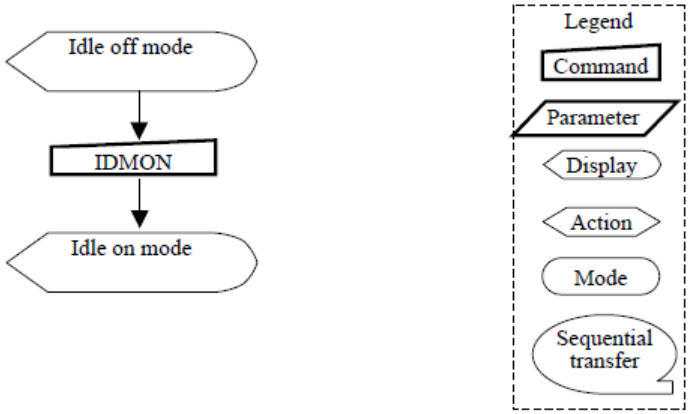
This command has no effect when module is already in idle off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
SW Reset	Idle Mode Off
HW Reset	Idle Mode Off

Flow Chart	

Idle off mode
IDMON
Idle on mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

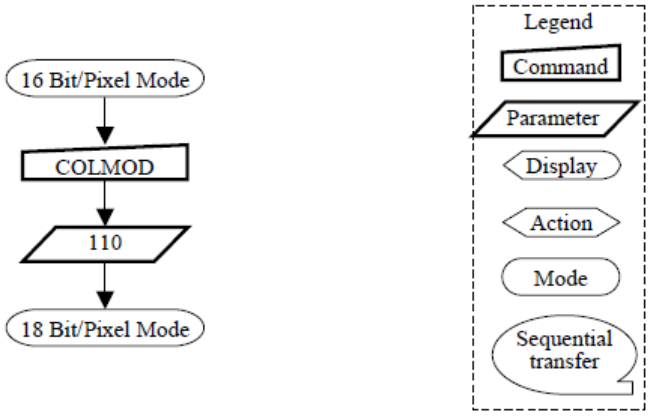
7.2.33. Interface Pixel Format (3Ah)

<table>
<tr><th>3A H</th><th colspan="20">COLMOD (Interface Pixel Format)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>B15</td><td>B14</td><td>B13</td><td>B12</td><td>B11</td><td>B10</td><td>B9</td><td>B8</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3A</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>D2</td><td>D1</td><td>D0</td><td>011,
101,
110,
111</td></tr>
<tr><td>Description</td><td colspan="20">This command is used to define the format of RGB picture data, which is to be transferred via the MCU Interface. The formats are shown in the table:

<table>
<tr><th>Control Interface Colour Format</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>Not Defined</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Not defined</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Not defined</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>12 bit/pixel</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Not Defined</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>16 bit/pixel</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>18 bit/pixel</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>24 bit/pixel</td><td>1</td><td>1</td><td>1</td></tr>
</table>

Note: In 12, 16 & 18 Bit/Pixel modes, the LUT is applied to transfer data into the Frame Memory.

X = don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="20">There is no visible effect until the Frame Memory is written to.</td></tr>
<tr><td>Register Availability</td><td colspan="20">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="20">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>24 bit/pixel</td></tr>
<tr><td>SW Reset</td><td>No Change</td></tr>
<tr><td>HW Reset</td><td>24 bit/pixel</td></tr>
</table>
</td></tr>
</table>

Flow Chart	

16 Bit/Pixel Mode
COLMOD
110
18 Bit/Pixel Mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

7.2.34. Read ID1 (DAh)

DA H	RDID1 (Read ID1)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	1	1	0	1	1	0	1	0	DA
1st parameter	1	↑	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
2nd parameter	1	↑	1	X	X	X	X	X	X	X	X	xx	xx	xx	xx	xx	xx	xx	xx	xx
Description	This read byte identifies the LCD module's manufacturer. X = Don't care																			
Restriction																				

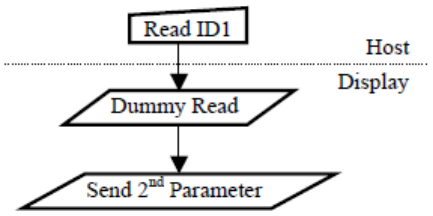
Register Availability

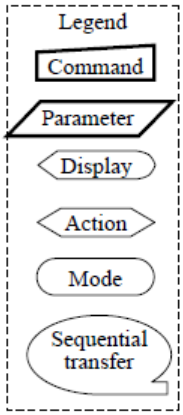
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	XX_{HEX}
SW Reset	XX_{HEX}
HW Reset	XX_{HEX}

Flow Chart





7.2.35. Read ID2 (DBh)

DB H	RDID2 (Read ID2)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	1	1	0	1	1	0	1	1	DB
1st parameter	1	↑	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
2nd parameter	1	↑	1	X	X	X	X	X	X	X	X	1	V6	V5	V4	V3	V2	V1	V0	80 … FF

Description

This read byte is used to track the LCD module/driver version. It is defined by display supplier (with end customer's agreement) and changes each time a revision is made to the display, material or construction specifications. See Table:

ID Byte Value V[6…0]	Version	Changes
80h		
81h		
82h		
83h		

X = Don't care

Restriction

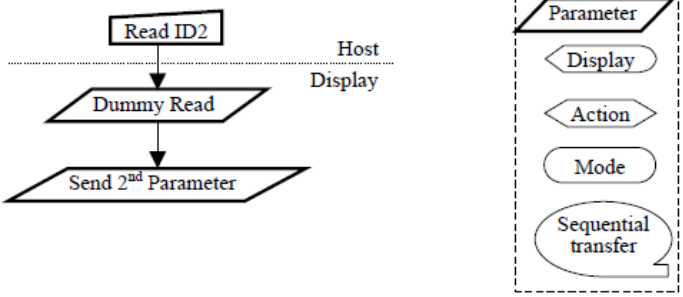
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	See Description
SW Reset	See Description
HW Reset	See Description

Flow Chart



7.2.36. Read ID3 (DCh)

DC H	RDID3 (Read ID3)																		
	D/CX	RDX	WRX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	HEX
Command	0	1	↑	X	X	X	X	X	X	X	X	1	1	0	1	1	1	0	0	DC
1st parameter	1	↑	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
2nd parameter	1	↑	1	X	X	X	X	X	X	X	X	xx	xx	xx	xx	xx	xx	xx	xx	xx
Description	This read byte identifies the LCD module/driver. X = Don't care																			
Restriction																				

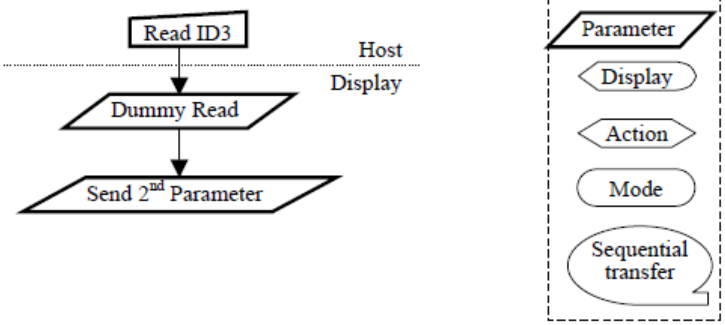
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	XX_{HEX}
SW Reset	XX_{HEX}
HW Reset	XX_{HEX}

Flow Chart



8. Functional Description

8.1. CPU Interface

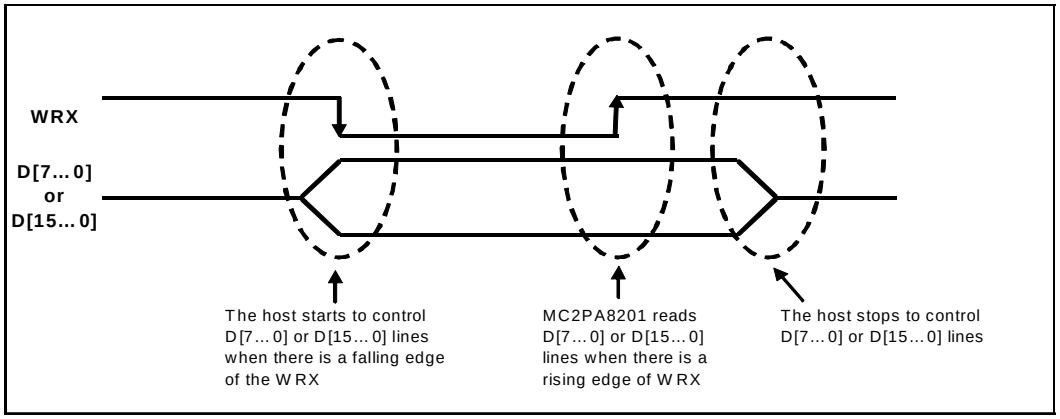
8.1.1. Parallel Interface

MC2PA8201 uses 11-wires 8-data parallel interface (16/8X = Low) or 19-wires 16-bit parallel interface (16/8X = High). The chip-select **CSX** (active low) enables and disables the parallel interface. **RESX** (active low) is an external reset signal. **WRX** is the parallel data write, **RDX** is the parallel data read and **D[7…0]** or **D[15…0]** is parallel data.
The Graphics Controller Chip reads the data at the rising edge of **WRX** signal. The D/CX is data/command flag. When D/CX = "1", D15 (or D7) to D0 bits are display RAM data or command parameters. When D/CX = "0" D15 (or D7) to D0 bits are commands.

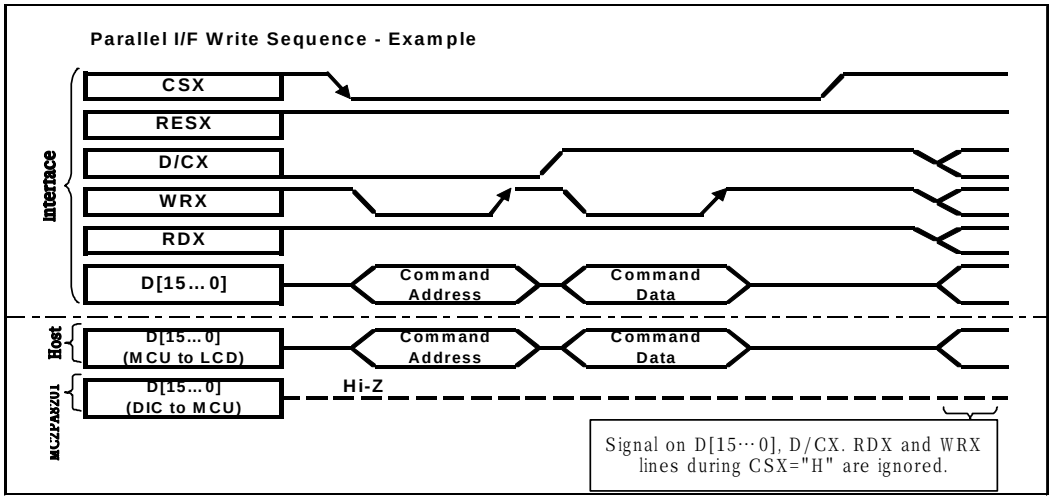
8.1.1.1. Write Cycle/Sequence

The write cycle means that the host writes information (command or/and data) to MC2PA8201 via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (D/CX, RDX, WRX) and 8 (D[7…0]) or 16 (D[15…0]) data signals. D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are a command if the control signal is low (= '0') and vice versa it is data (= '1').

The write cycle is described in the following figure.



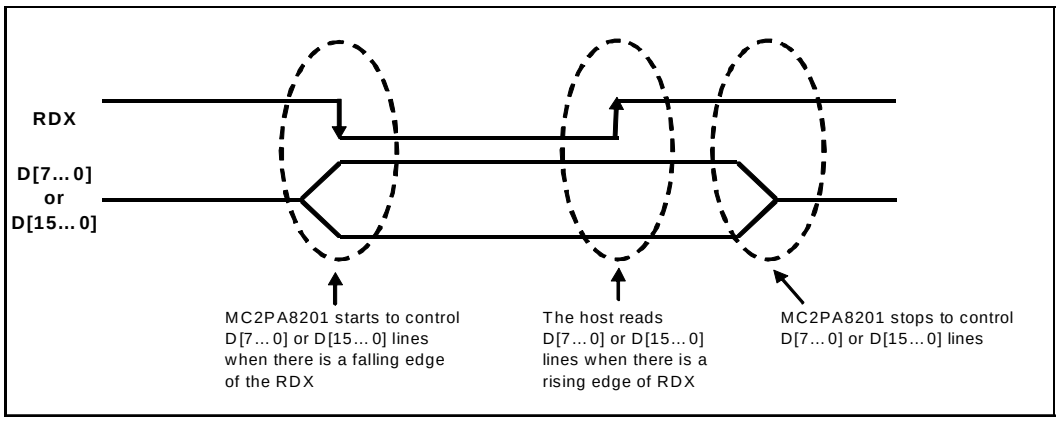
Note: WRX is an unsynchronized signal (It can be stopped).



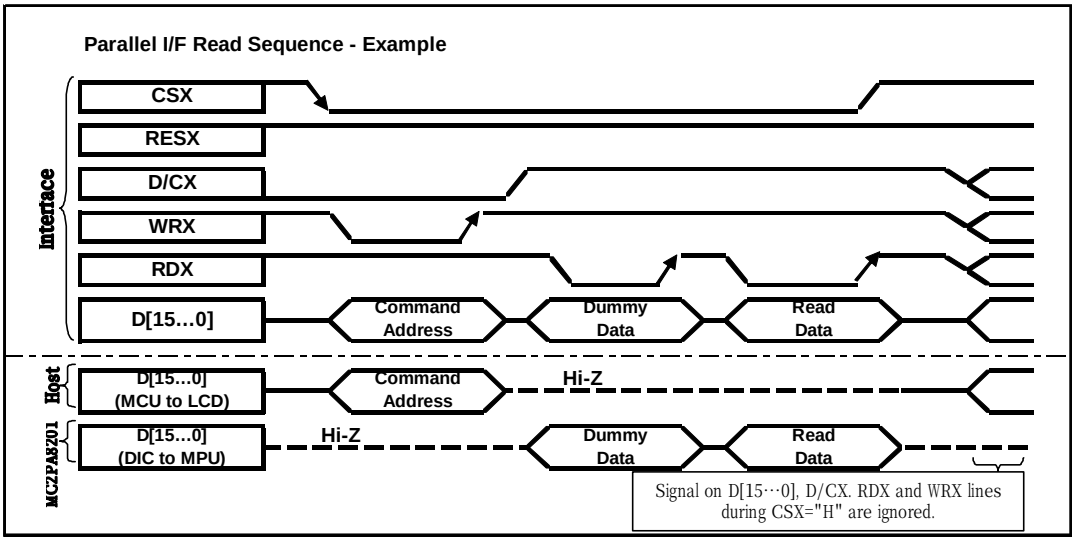
8.1.1.2. Read Cycle/Sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from MC2PA8201 via interface. The display with MC2PA8201 sends data (D[7…0] or D[15…0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

The RDX cycle is described in the following figure.



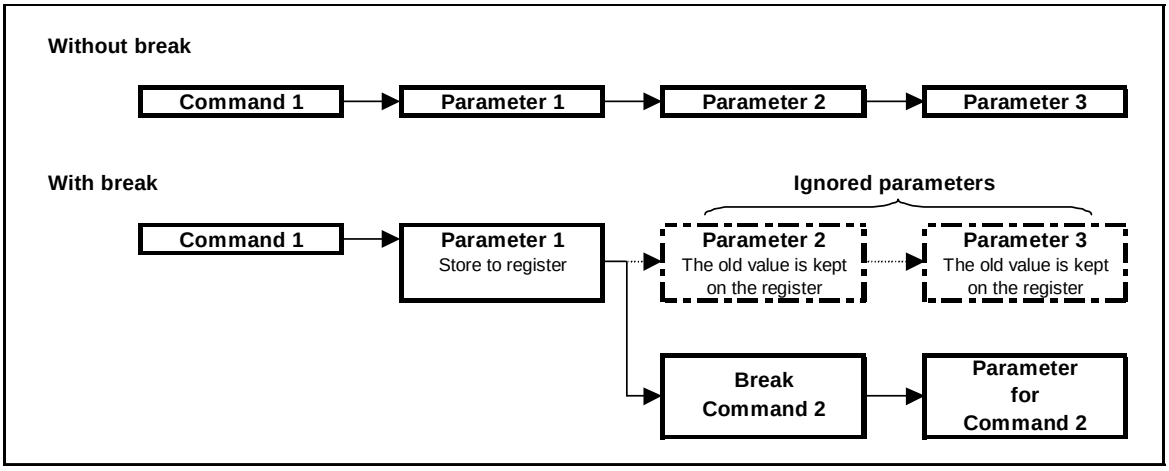
Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read Data is only valid when D/CX input is set High, if D/CX is set Low during read then Driver Data line will be High Impedance.

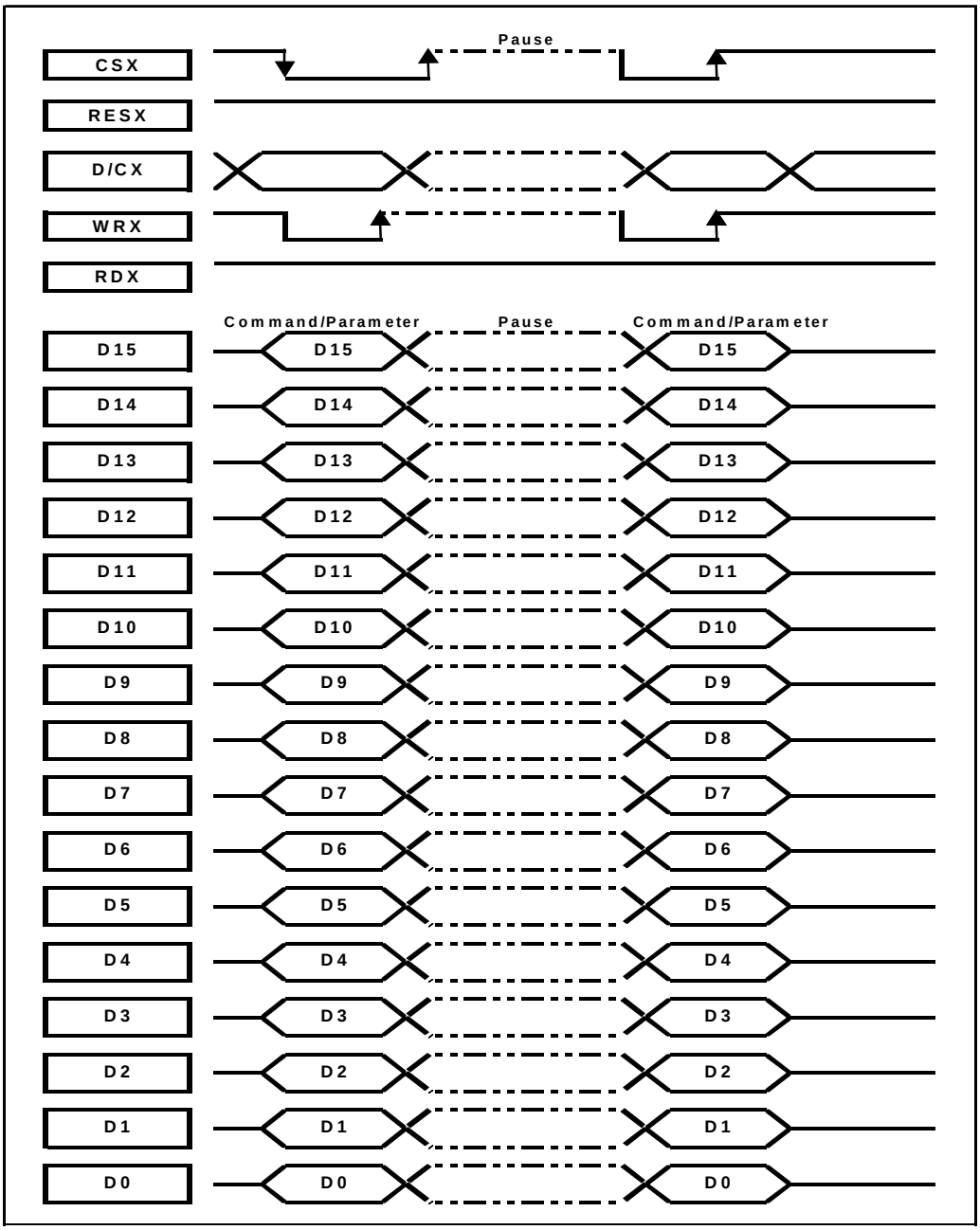
8.1.2. MC2PA8201 Data Transfer Break

If a 1 or more parameter command is being sent and a break occurs sending before the last parameter of the command and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameters after the break occurred is rejected if there is a new command as shown in the following example:-



Break can be e.g. another command or noise pulse.

8.1.3. MC2PA8201 Data Transfer Pause



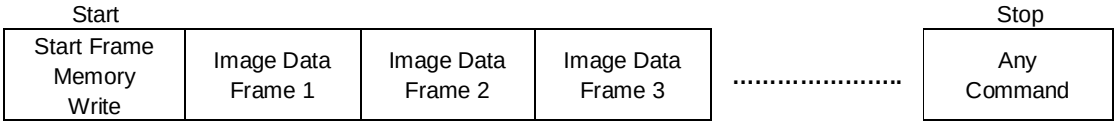
This applies to the following 4 conditions:
1. Command-Pause-Command
2. Command-Pause-Parameter
3. Parameter-Pause-Command
4. Parameter-Pause-Parameter

8.1.4. MC2PA8201 Data Transfer Mode

MC2PA8201 has four colour modes for transferring data to the display RAM. These are 12-bit colour per pixel, 16-bit colour per pixel, 18-bit colour per pixel and 24-bit colour per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

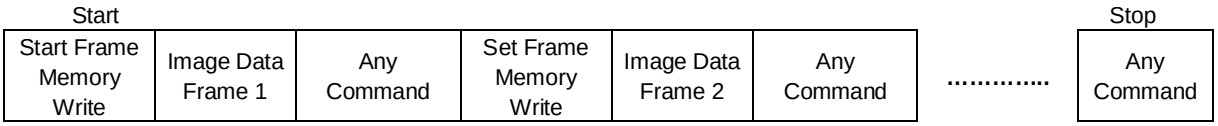
8.1.4.1. Method 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.



8.1.4.2. Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.

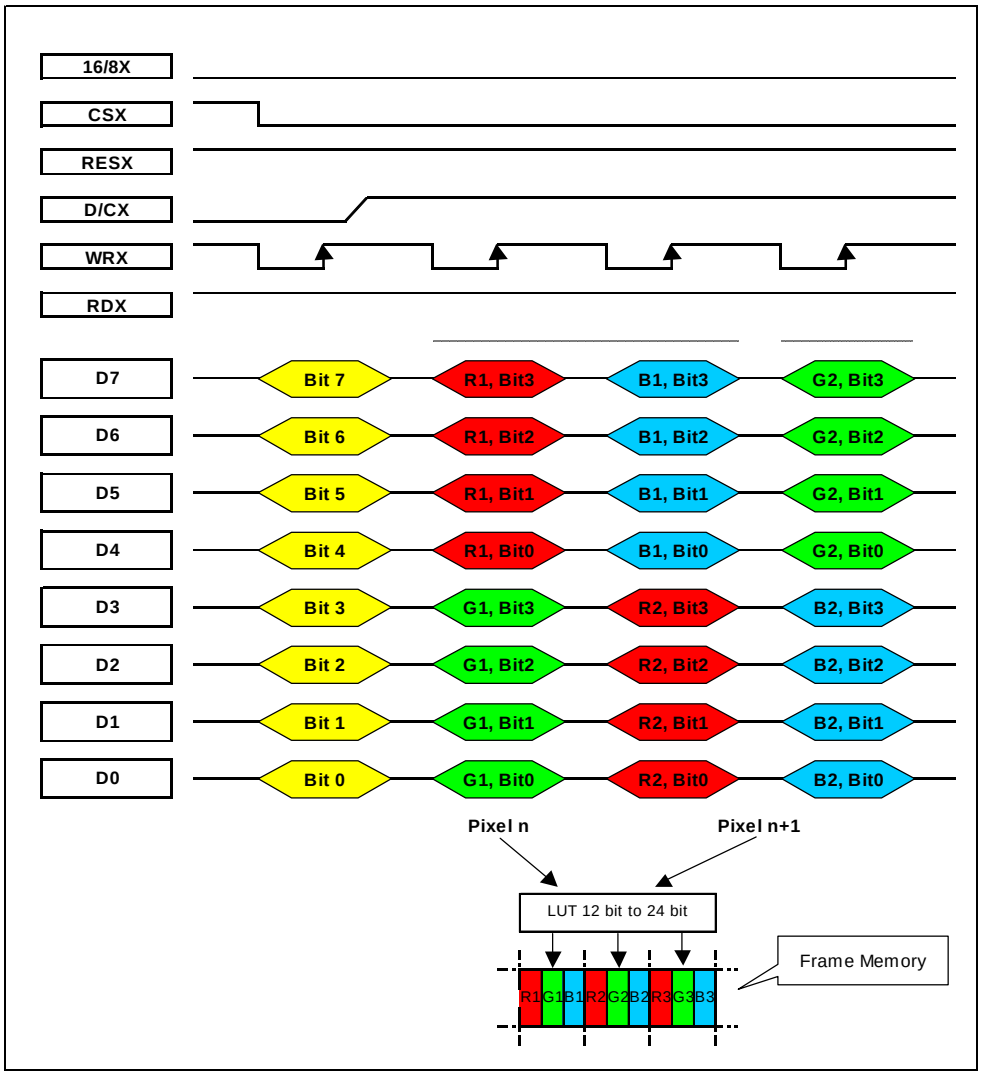


Note:
1. These apply to all Data Transfer Colour modes on Parallel interface.
2. The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored in the Frame Memory.

8.1.5. MC2PA8201 Data Colour Coding

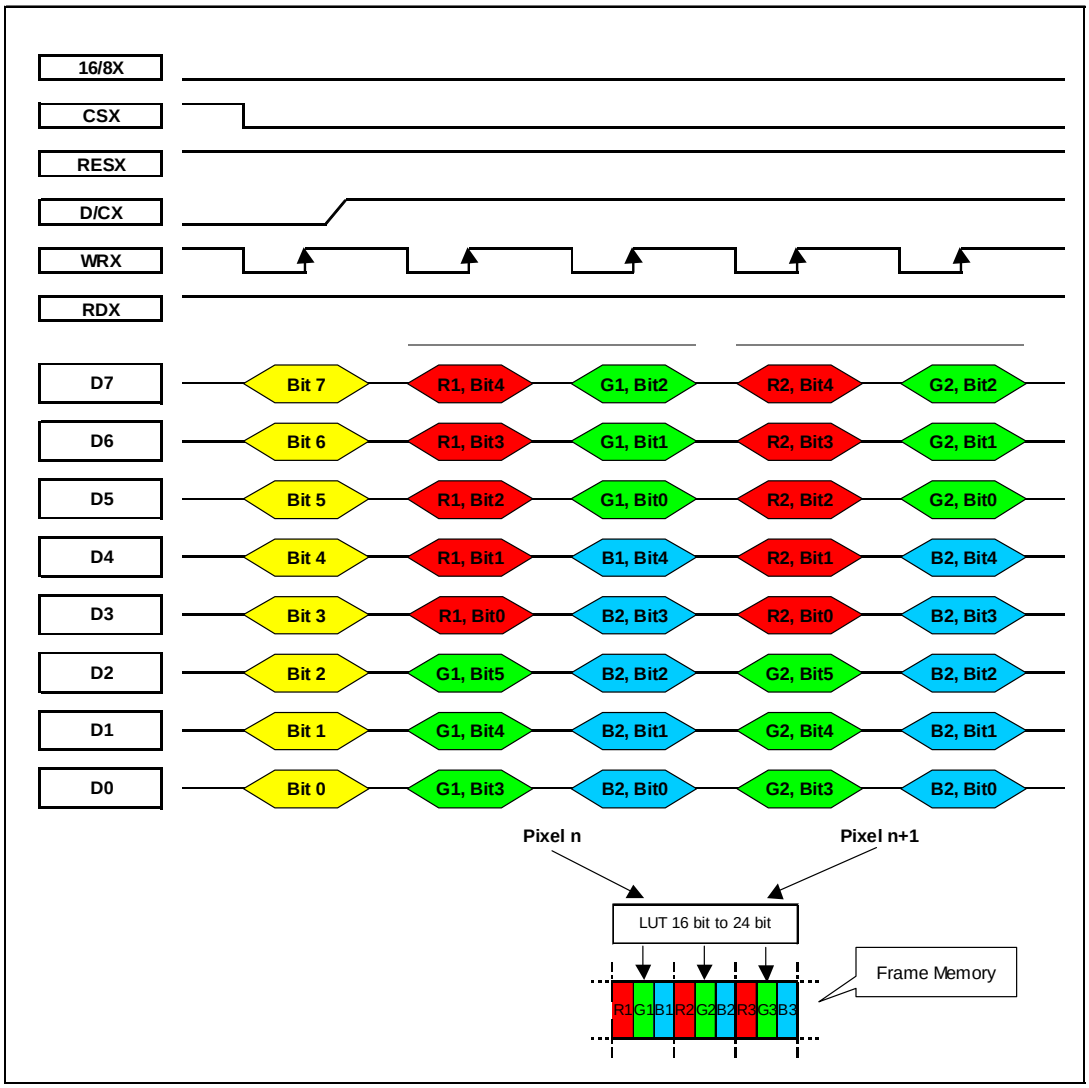
8.1.5.1. 8 Data Line Parallel

8.1.5.1.1. 12 bit/pixel (R 4-bit, G 4-bit, B 4-bit), 4,096 colours



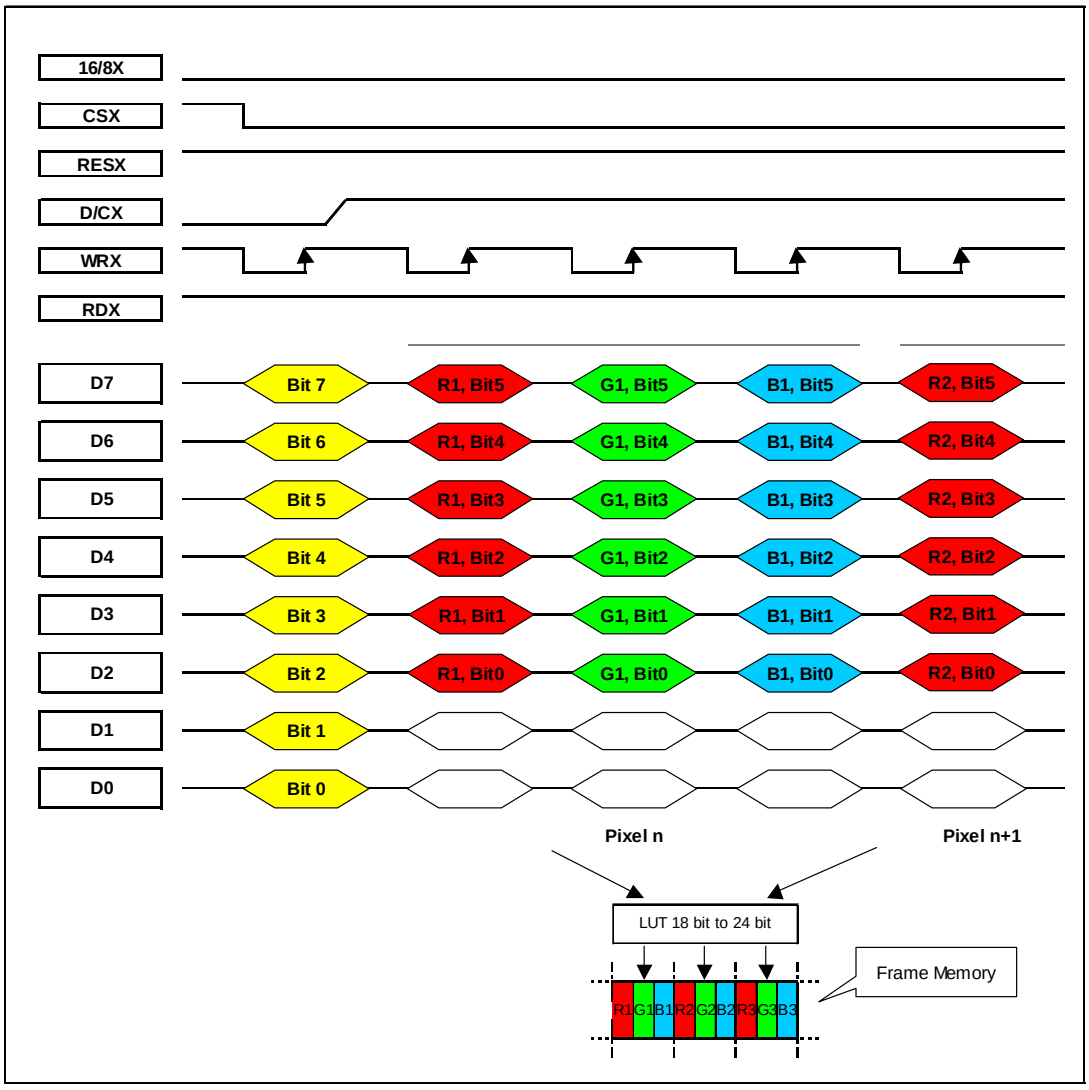
Note: The Data order is as follows, MSB = D7, LSB = D0 and Picture Data is MSB = Bit3, LSB = Bit0 for Red, Green and Blue data.

8.1.5.1.2. 16 bit/pixel (R 5-bit, G 6-bit, B 5-bit), 65,536 colours



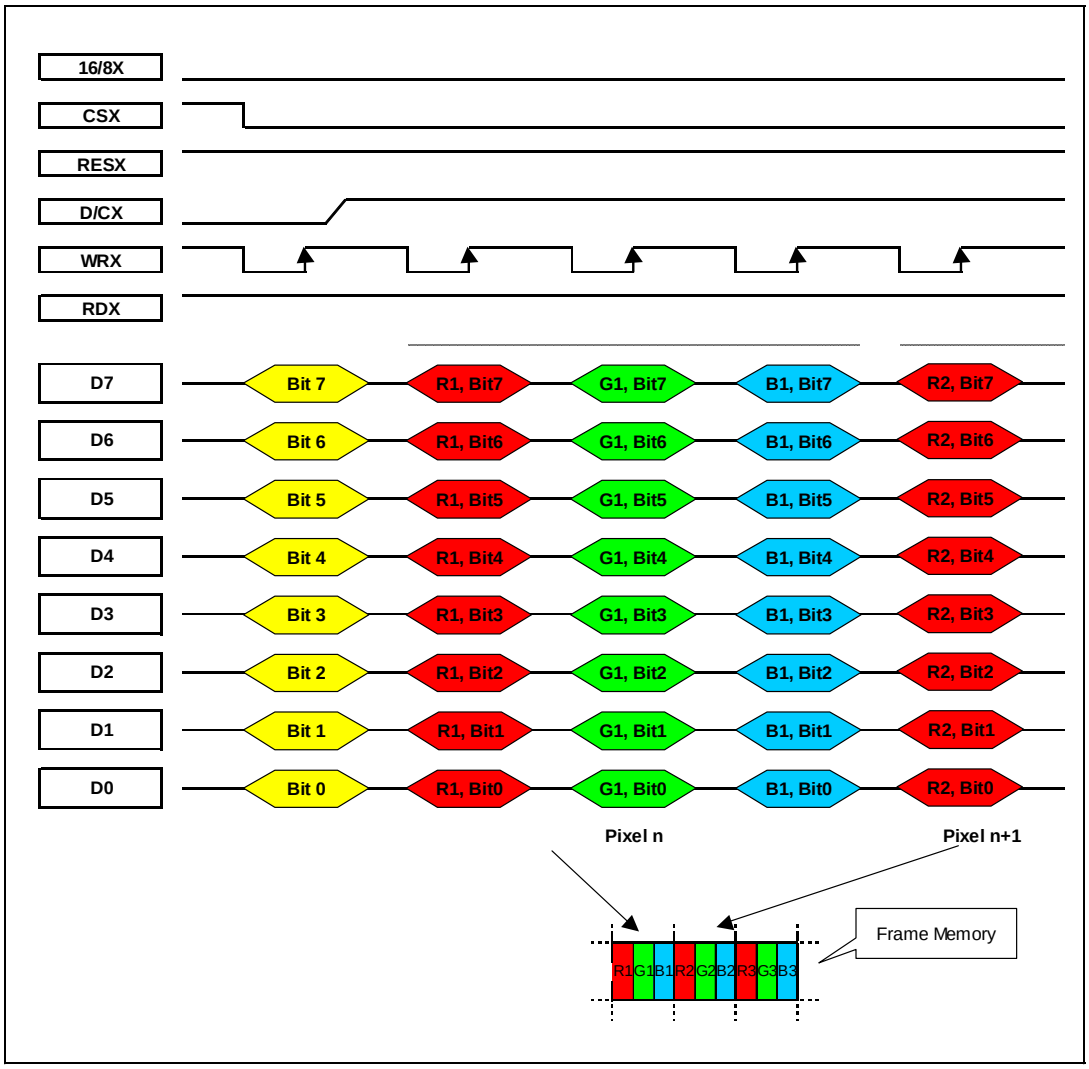
Note: The Data order is as follows, MSB = D7, LSB = D0 and Picture Data is MSB = Bit5, LSB = Bit0 for Green data and MSB = Bit4, LSB = Bit0 for Red and Blue data.

8.1.5.1.3. 18 bit/pixel (R 6-bit, G 6-bit, B 6-bit), 262,144 colours



Note: The Data order is as follows, MSB = D7, LSB = D0 and Picture Data is MSB = Bit5, LSB = Bit0 for Red, Green and Blue data.

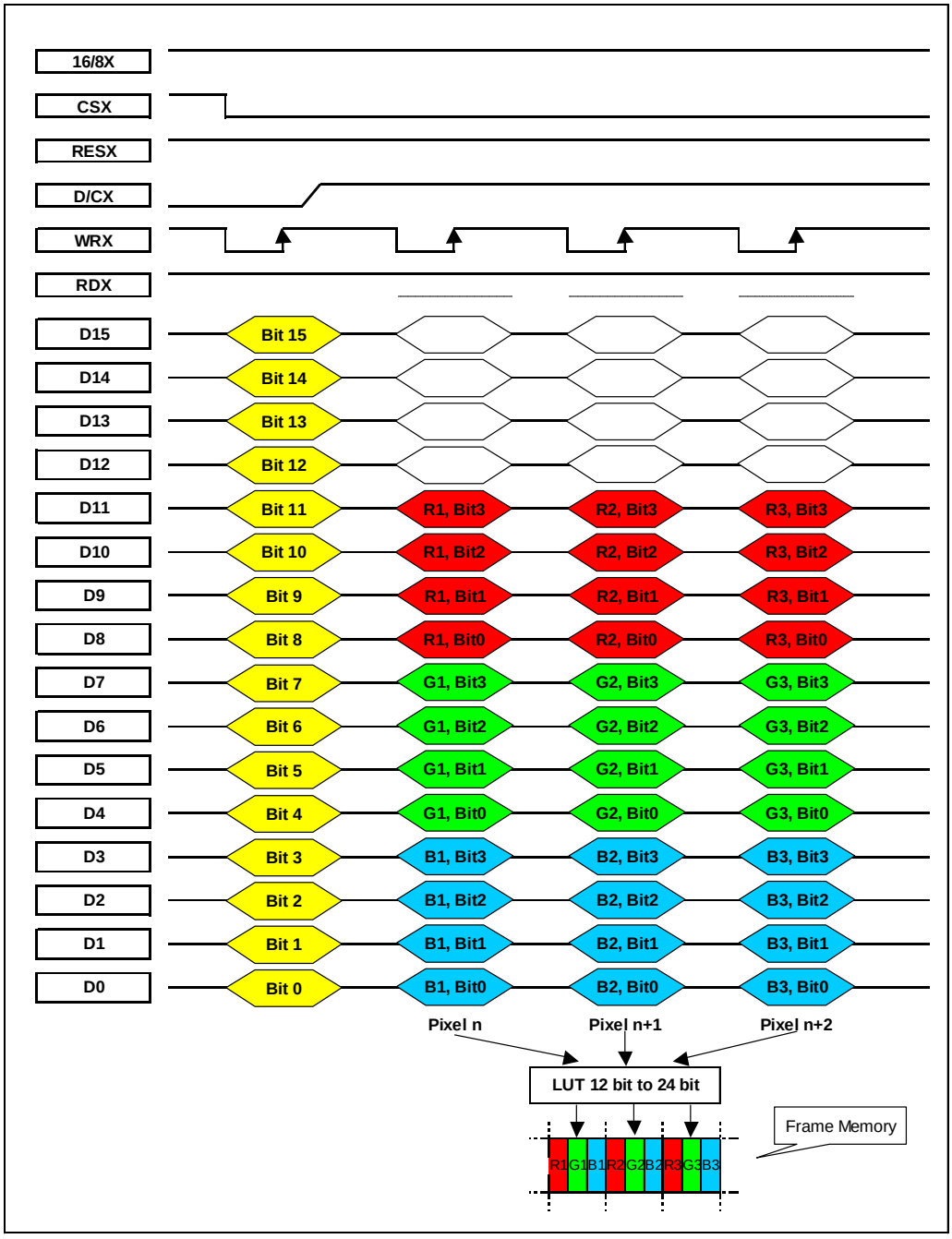
8.1.5.1.4. 24 bit/pixel (R 8-bit, G 8-bit, B 8-bit), 16,777,216 colours



Note: The Data order is as follows, MSB = D7, LSB = D0 and Picture Data is MSB = Bit7, LSB = Bit0 for Red, Green and Blue data.

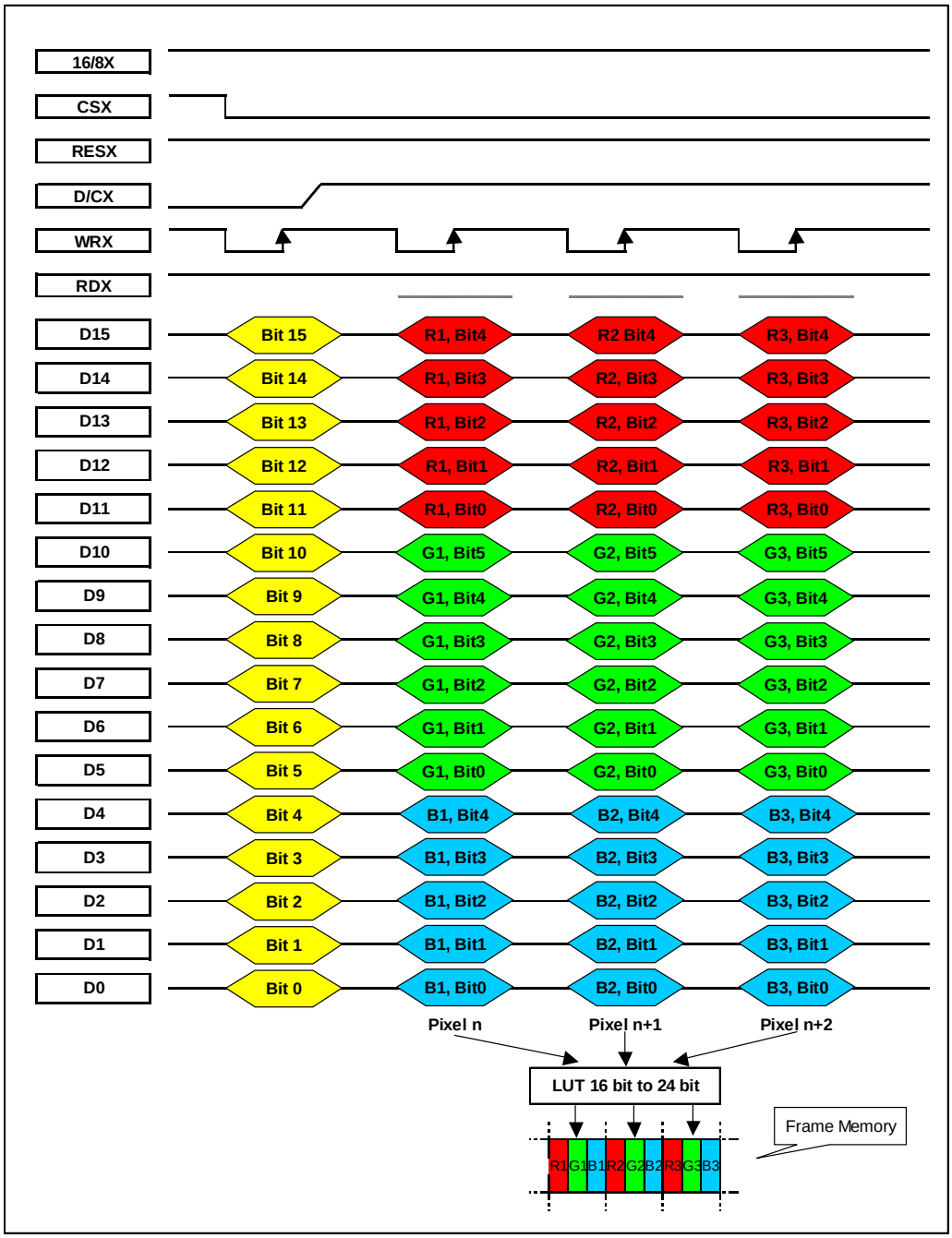
8.1.5.2. 16. Data Line Parallel

8.1.5.2.1. 12 bit/pixel (R 4-bit, G 4-bit, B 4-bit), 4,096 colours



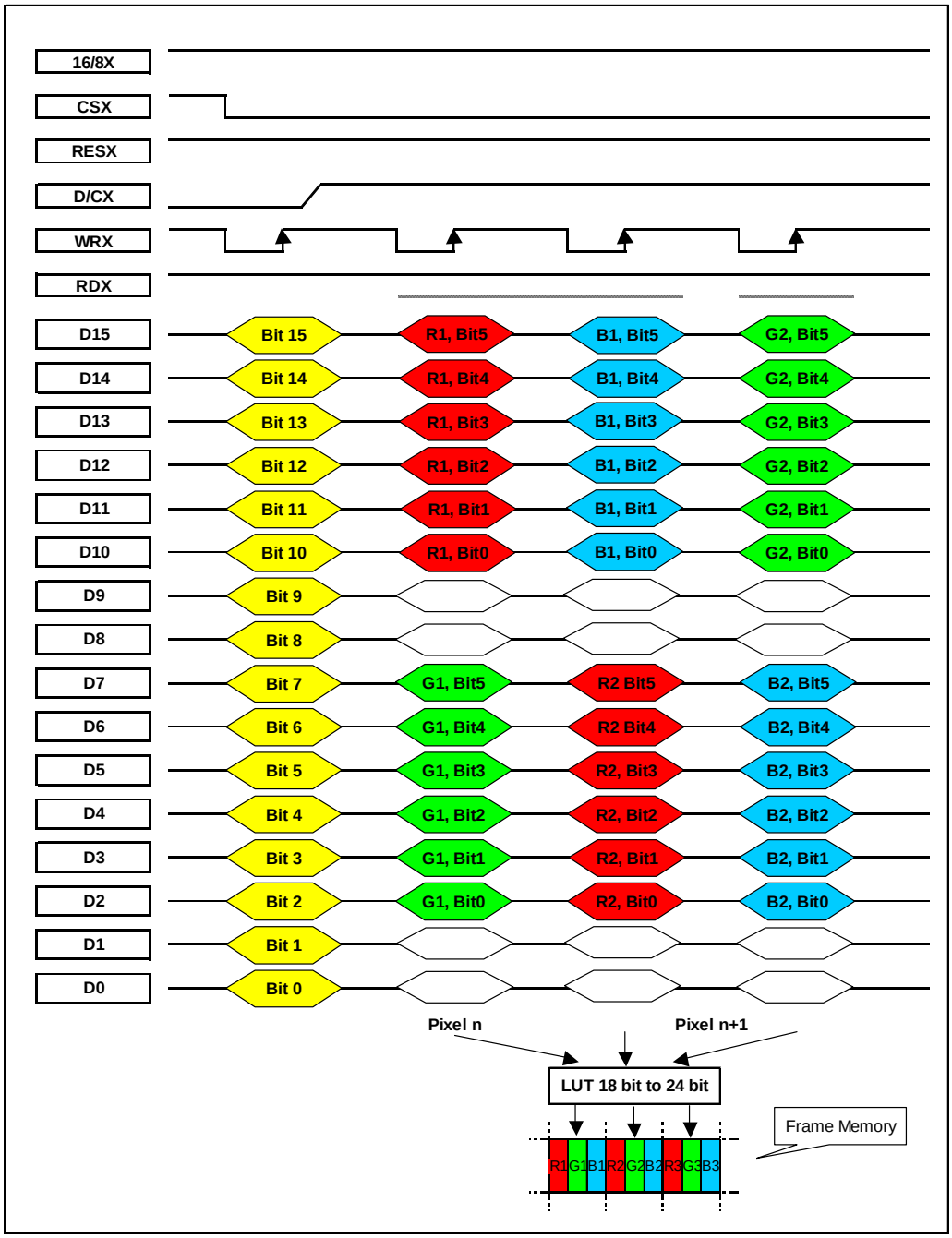
Note: The Data order is as follows, MSB = D15, LSB = D0 and Picture Data is MSB = Bit3, LSB = Bit0 for Red, Green and Blue data.

8.1.5.2.2. 16 bit/pixel (R 5-bit, G 6-bit, B 5-bit), 65,536 colours



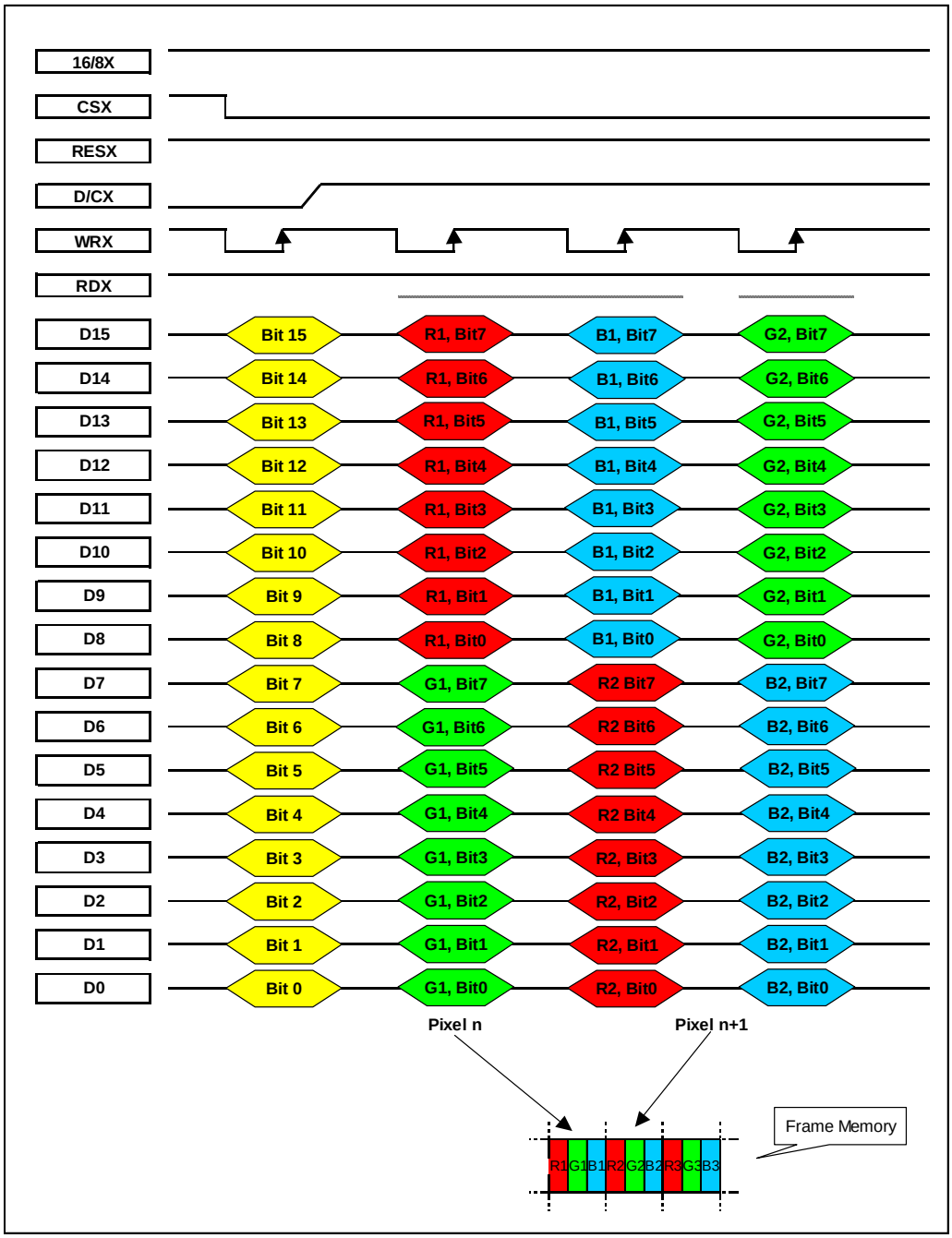
Note: The Data order is as follows, MSB = D15, LSB = D0 and Picture Data is MSB = Bit5, LSB = Bit0 for Green data and MSB = Bit4, LSB = Bit0 for Red and Blue data.

8.1.5.2.3. 18 bit/pixel (R 6-bit, G 6-bit, B 6-bit), 262,144 colours



Note: The Data order is as follows, MSB = D15, LSB = D0 and Picture Data is MSB = Bit5, LSB = Bit0 for Red, Green and Blue data.

8.1.5.2.4. 24 bit/pixel (R 8-bit, G 8-bit, B 8-bit), 16,777,216 colours

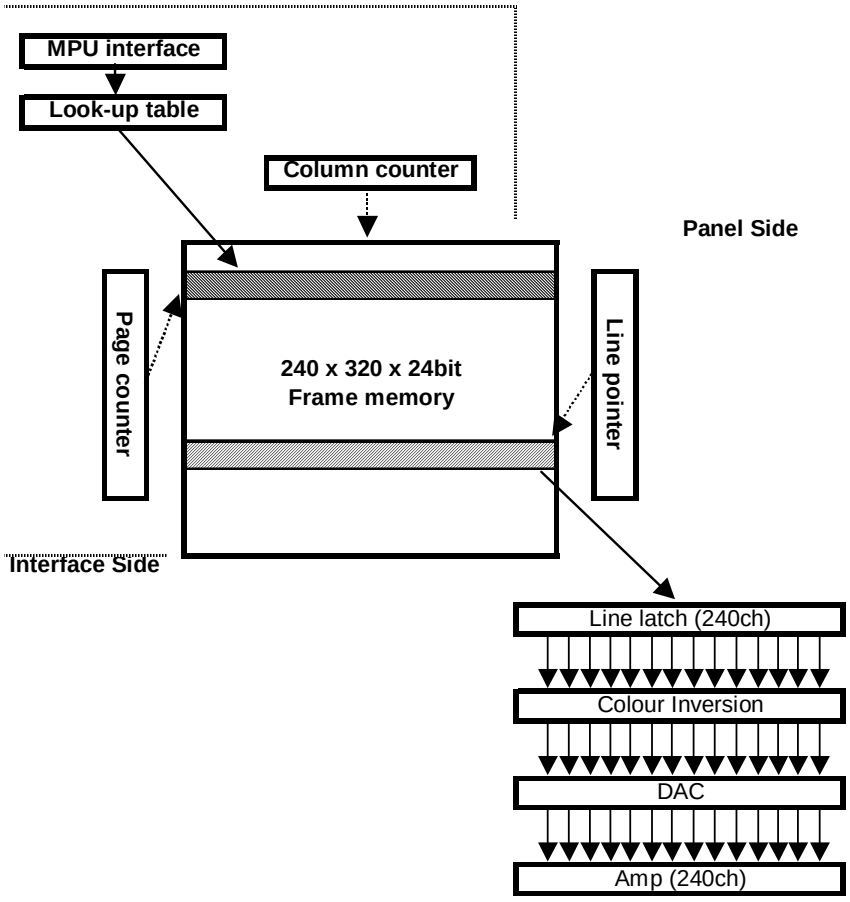


Note: The Data order is as follows, MSB = D15, LSB = D0 and Picture Data is MSB = Bit7, LSB = Bit0 for Red, Green and Blue data.

8.2. Display Data RAM

8.2.1. Configuration

The display data RAM stores display dots and consists of 1,843,200 bits (240x24x320 bits).
There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC.
There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

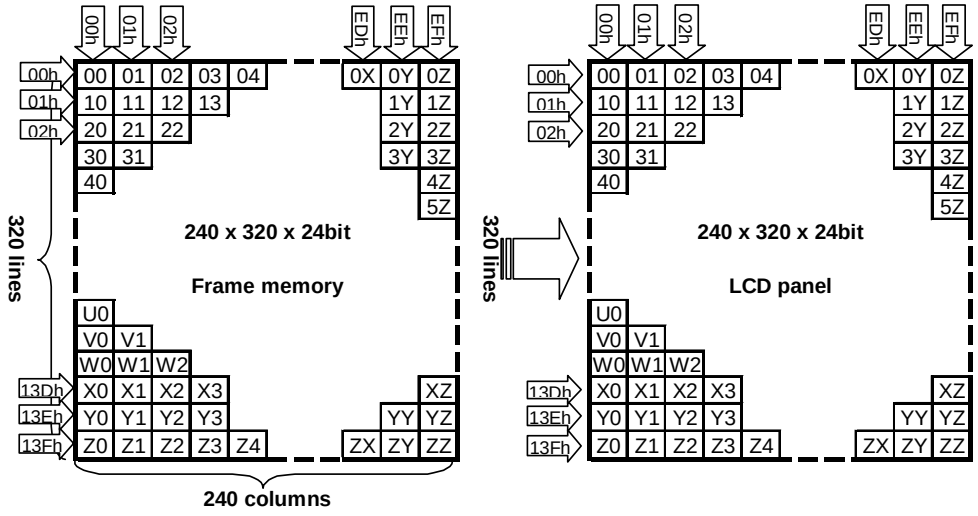


8.2.2. Memory to Display Address Mapping

8.2.2.1. Normal Display On or Partial Mode On, Vertical Scroll Off

In this mode, content of the frame memory within an area where column pointer is 0000h to 00EFh and page pointer is 0000h to 013Fh is displayed.
To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0).

8.2.2.1. Normal Display On or Partial Mode On, Vertical Scroll Off

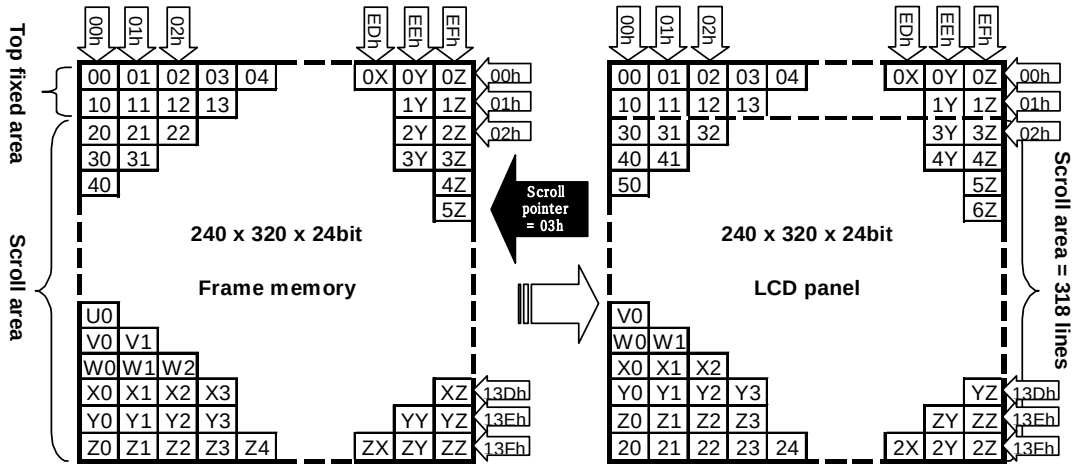


8.2.2.2 Vertical Scroll Mode

There is a vertical scrolling mode, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

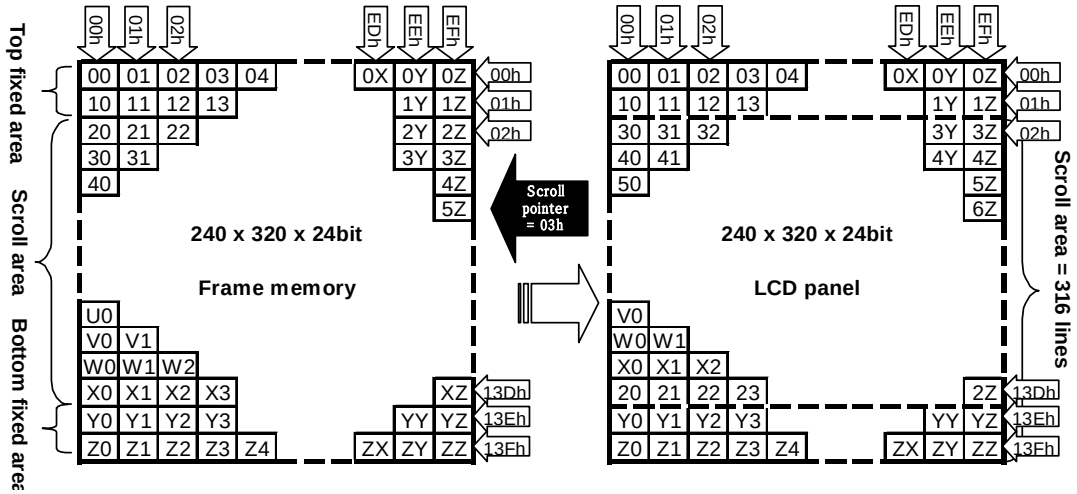
Example 1

TFA=2, VSA=318, BFA=0 when MADCTL Bit B4=0



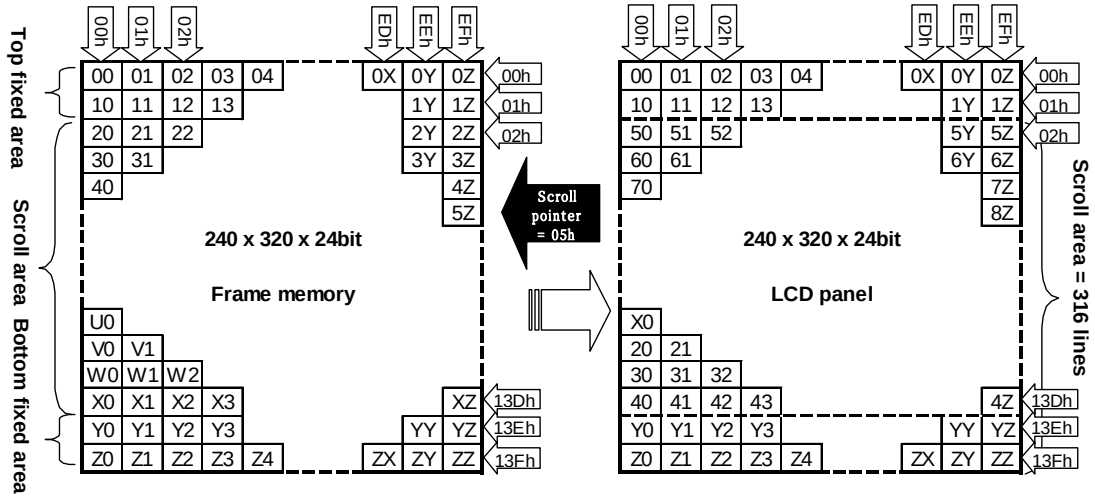
Example 2

TFA=2, VSA=316, BFA=2 when MADCTL Bit B4=0



Example 3

TFA=2, VSA=316, BFA=2 when MADCTL Bit B4=0



Note: When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)≠320, Scrolling Mode is undefined.

8.2.2.3. Vertical Scroll example

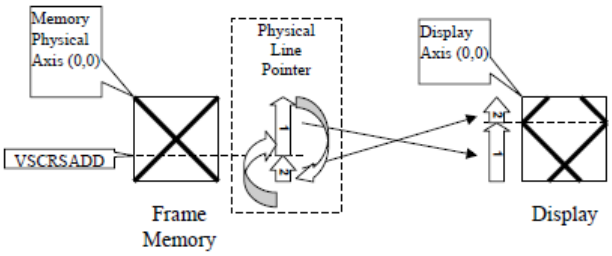
8.2.2.3.1. Case 1: TFA+VSA+BFA<320

N/A. Do not set TFA+VSA+BFA<320, unless unexpected picture will be shown.

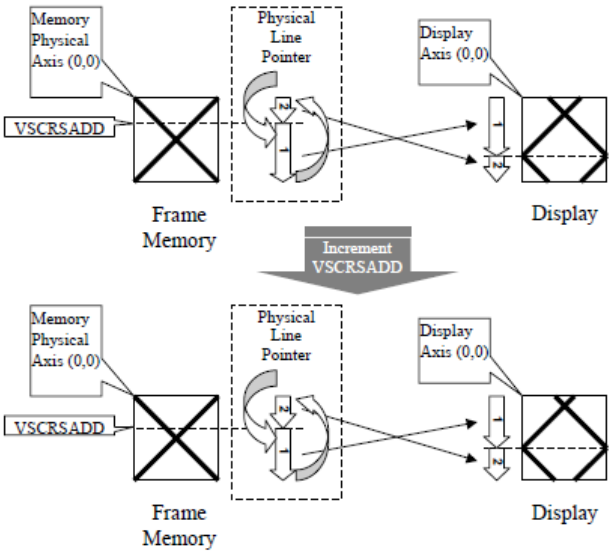
8.2.2.3.2. Case 2: TFA+VSA+BFA=320 (Rolling Scrolling)

Example 2-a. When TFA=0, VSA=320, BFA=0 and VSCRSADD=40.

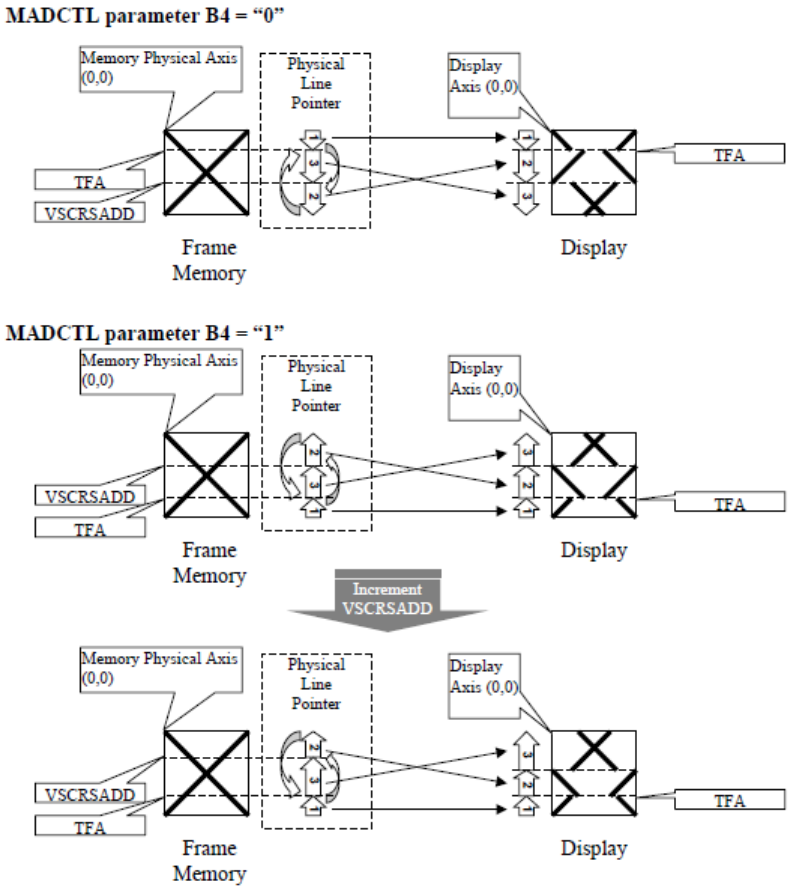
MADCTL parameter B4 = "1"



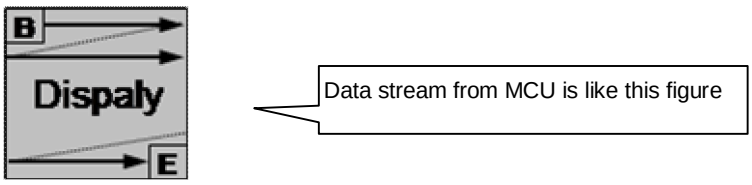
MADCTL parameter B4 = "0"



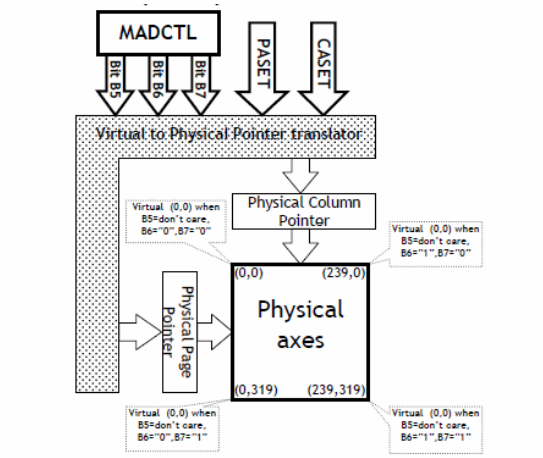
Example 2-b. When TFA=30, VSA=290, BFA=0 and VSCRSADD=80.



8.2.3. MCU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, Bits B5, B6, B7 as described below.



B5	B6	B7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319-Physical Page Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (239-Physical Column Pointer)	Direct to (319-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (319-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (319-Physical Page Pointer)	Direct to (239-Physical Column Pointer)

For each image orientation, the controls for the column and page counters apply as below: -

Table 8.3.3

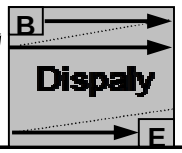
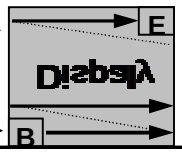
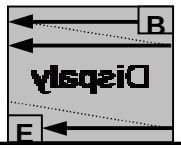
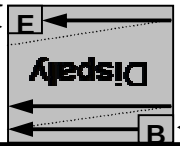
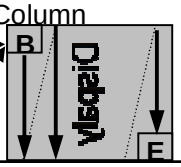
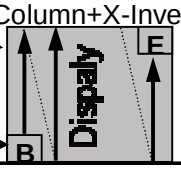
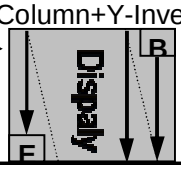
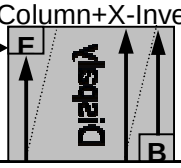
Condition	Column Counter	Page Counter
When RAMWR/RAMRD command is accepted.	Return to “Start Column”	Return to “Start Page”
Complete Pixel Read/Write action	Increment by 1	No change
The Column counter value is larger than “End column.”	Return to “Start Column”	Increment by 1
The Column counter value is larger than “End column” and the Page counter value is larger than “End page”.	Return to “Start Column”	Return to “Start Page”

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5. The write order for each pixel unit is

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

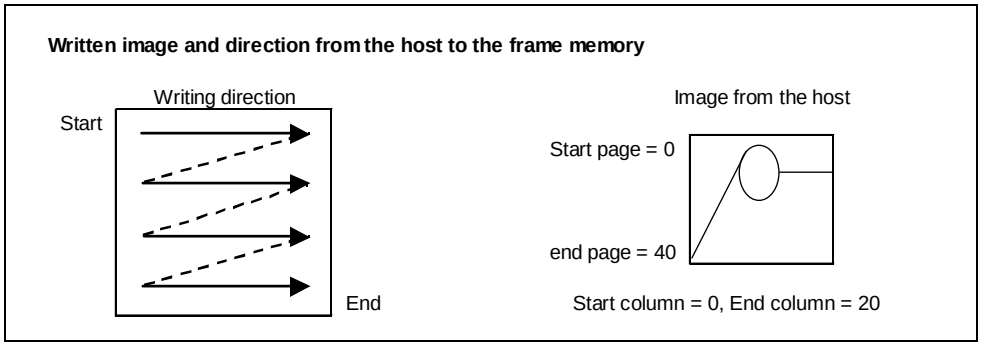
The resultant image for each orientation setting is illustrated below:

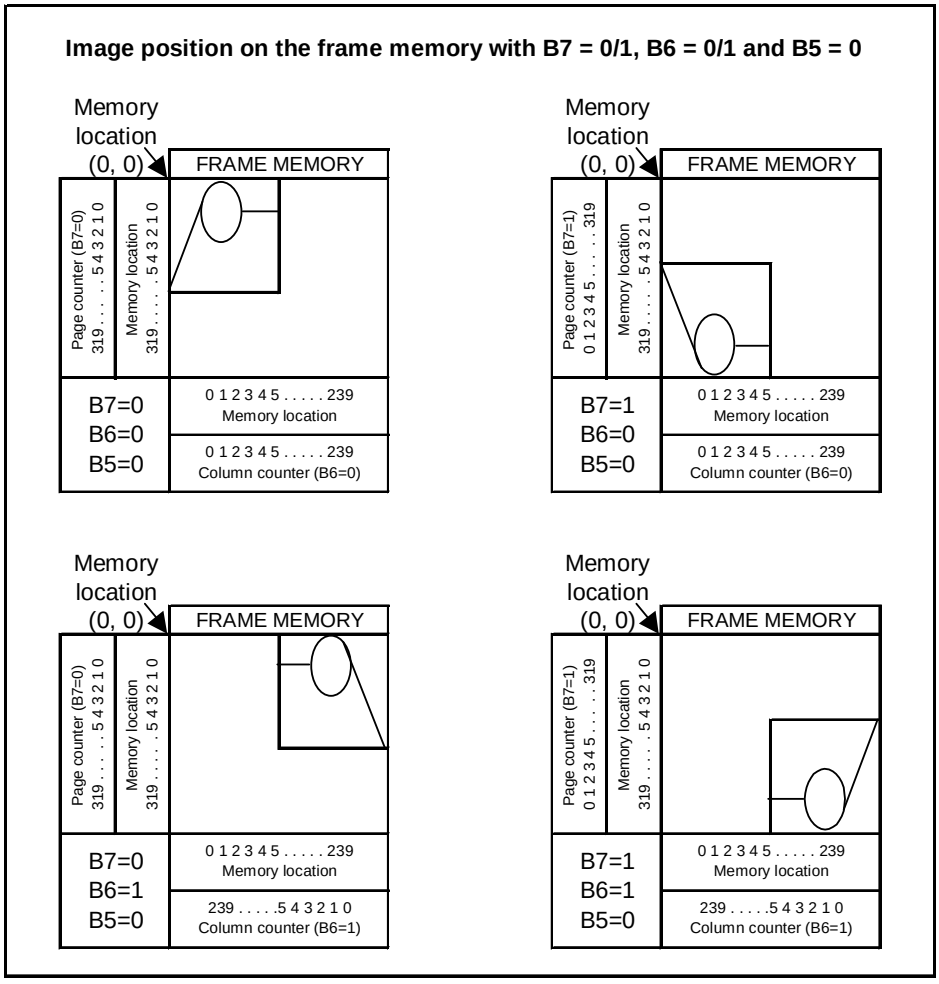
Image in Frame Memory	B5	B6	B7
Normal Memory(0, Command(0, 	0	0	0
Y-Invert Memory(0, Command(0,0 	0	0	1
X-Invert Memory(0, Command(0,0 	0	1	0
X-Invert+Y-Invert Memory(0, Command(0,0 	0	1	1
Exchange Row-Column Memory(0, Command(0, 	1	0	0
Exchange Row-Column+X-Invert(270 deg rotation) Memory(0, Command(0, 	1	0	1
Exchange Row-Column+Y-Invert(90 deg rotation) Memory(0, Command(0,0 	1	1	0
Exchange Row-Column+X-Invert+Y-Invert Memory(0, Command(0,0 	1	1	1

Example for rotation with B7, B6 and B5

This example is using following values: start page = 0, end page = 40, start column = 0 and end column = 20
=> *commands: page address set (0, 40) and column address set (0, 20).*

The sent figure is as follows and its sending order is as follows.





Written image and direction from the host to the frame memory

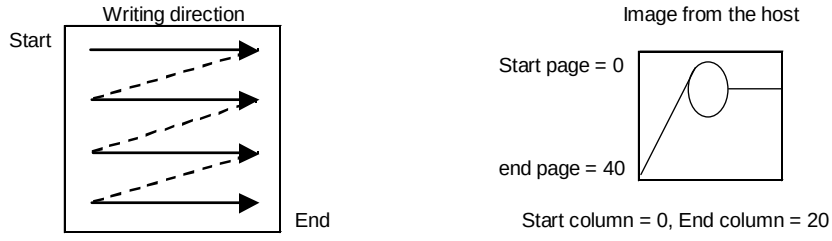
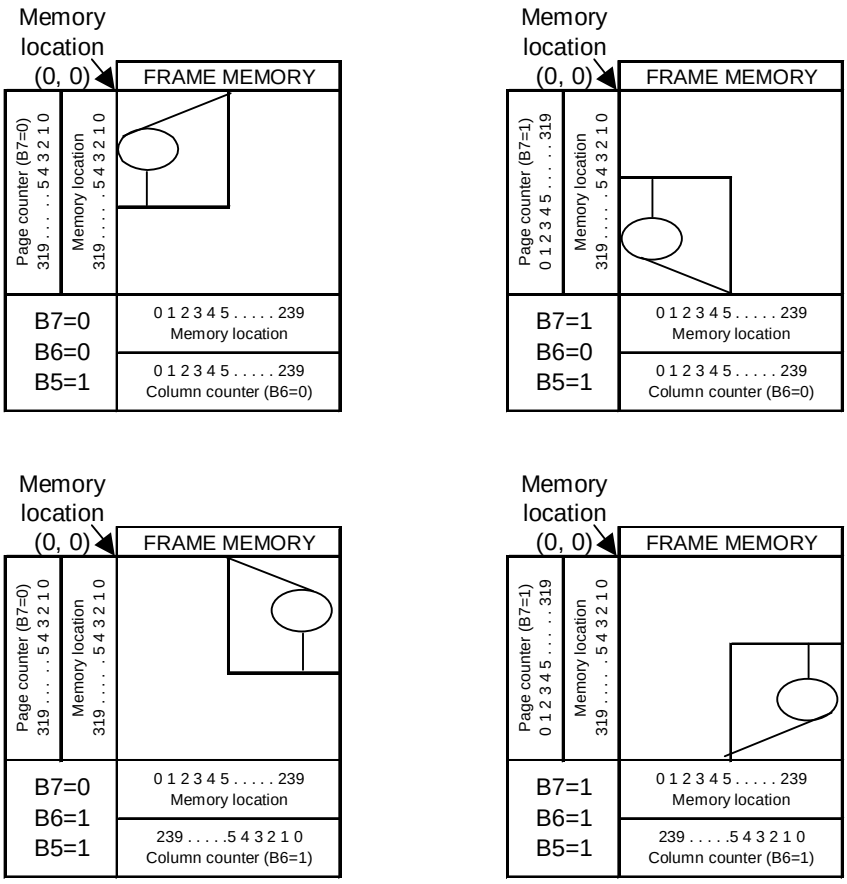


Image position on the frame memory with B7 = 0/1, B6 = 0/1 and B5 = 1

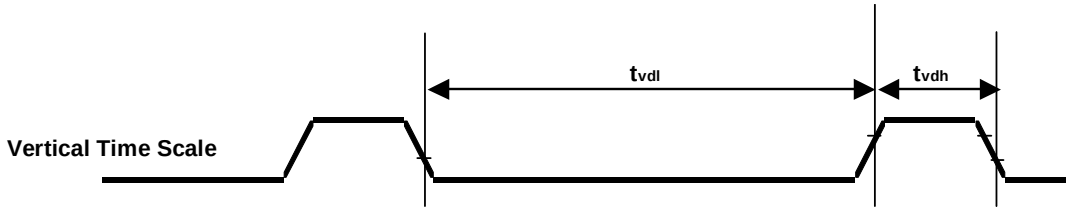


8.3. Tearing Effect Output Line

The Tearing Effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command.
The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

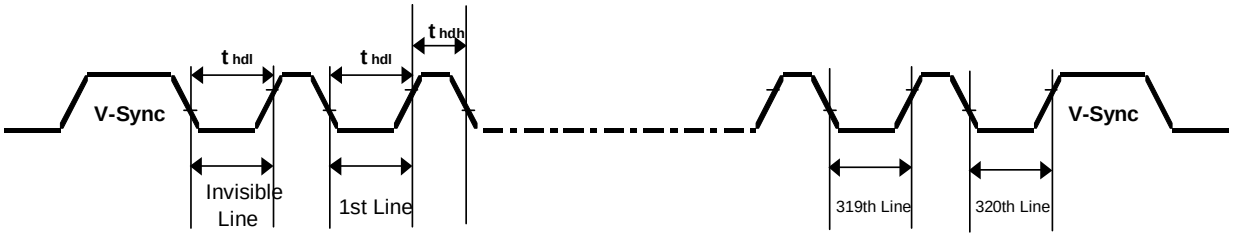
8.3.1. Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Sync information only:

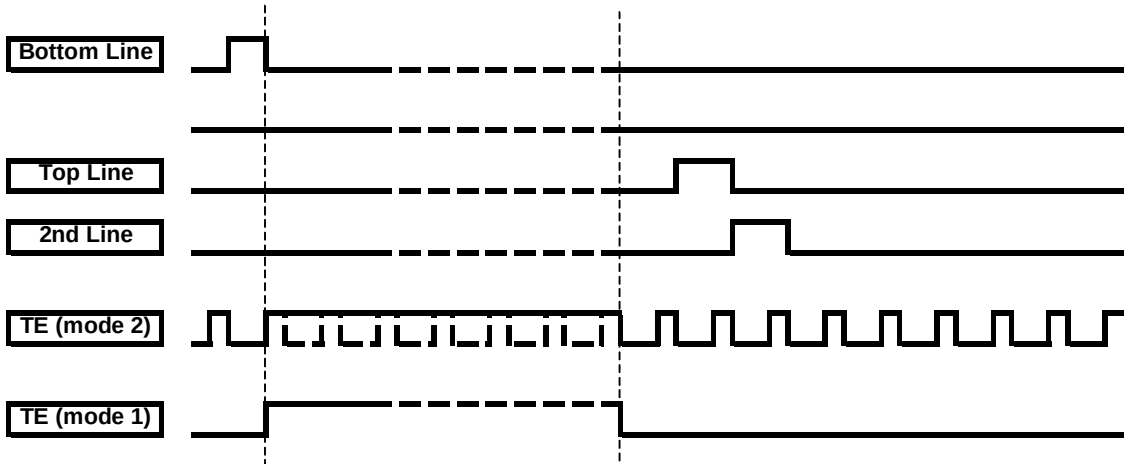


tvdh = The LCD display is not updated from the Frame Memory.
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2, the Tearing Effect Output signal consists of V-Sync and H-Sync information. There is one V-sync and 320 H-sync pulses per field:



thdh = The LCD display is not updated from the Frame Memory.
thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see above).



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

8.3.2. Tearing Effect Line Timings

The Tearing Effect signal is described below:

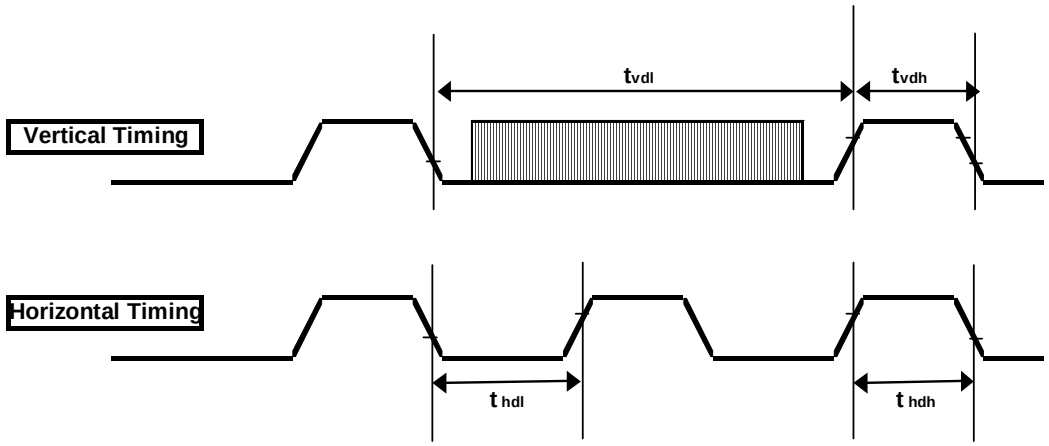
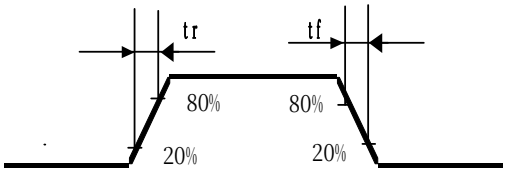


Table 8.4.1. AC characteristics of Tearing Effect Signal
Idle Mode Off/On (Frame Rate = 60.5Hz)

Symbol	Parameter	Min.	Max.	unit	Description
tvdl	Vertical Timing Low Duration	TBD	-	ms	
tvdh	Vertical Timing High Duration	1000	-	us	
thdl	Horizontal Timing Low Duration	TBD	-	us	
thdh	Horizontal Timing High Duration	TBD	500	us	

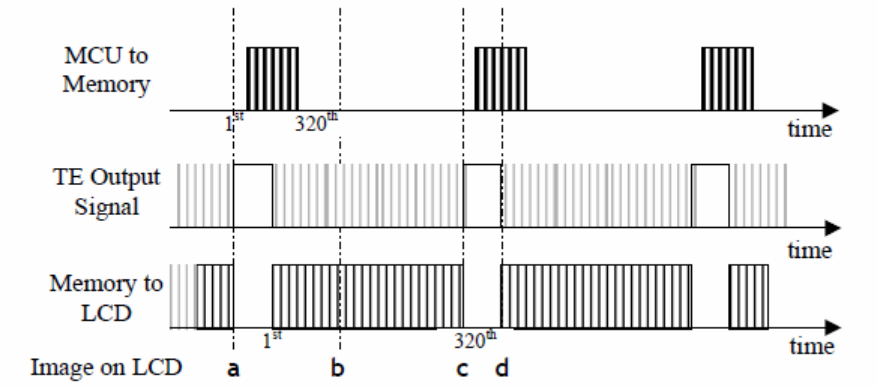
Notes:
1. The timings in Table 8.4.1 apply when MADCTL B4=0 and B4=1
2. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

Figure 8.4 Rise and fall times

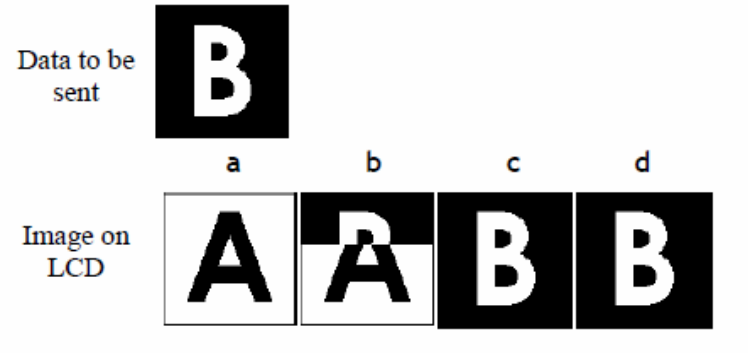


The Tearing Effect Output Line is fed back to the MCU and should be used as shown below to avoid Tearing Effect:

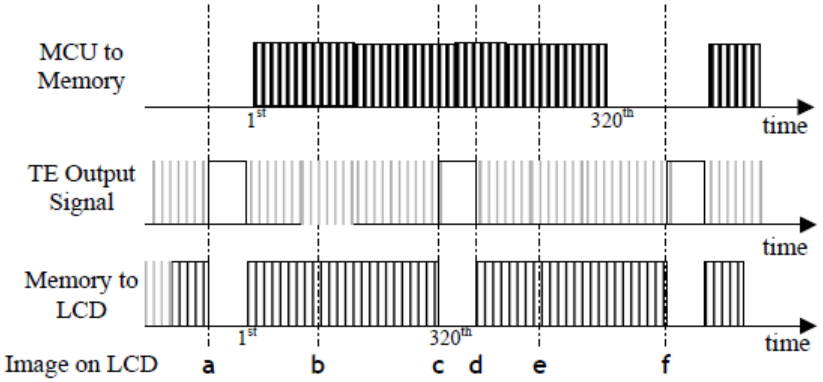
8.3.3. Example 1 MCU Write is faster than Panel Read.



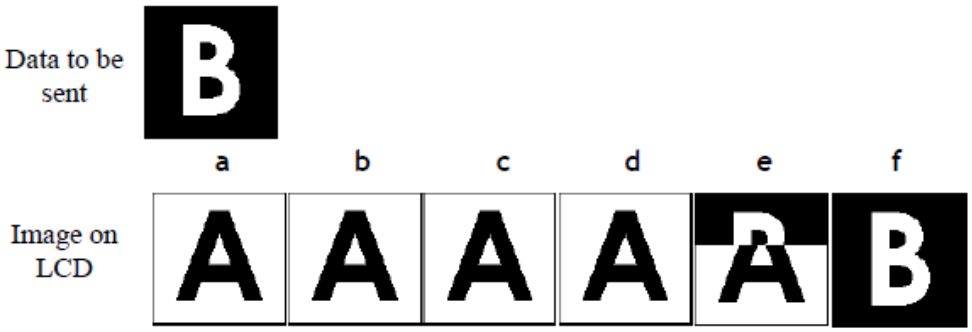
Data write to Frame Memory is now synchronized to the Panel Scan. I t should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



8.3.4. Example 2 MCU Write is Slower than Panel Read.



The MCU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MCU to Frame memory write position.



8.4. Preset Values

Display module suppliers can set preset values on their production line for optimum point individually for each display module with MC2PA8201.

8.5. Power ON/OFF Sequence

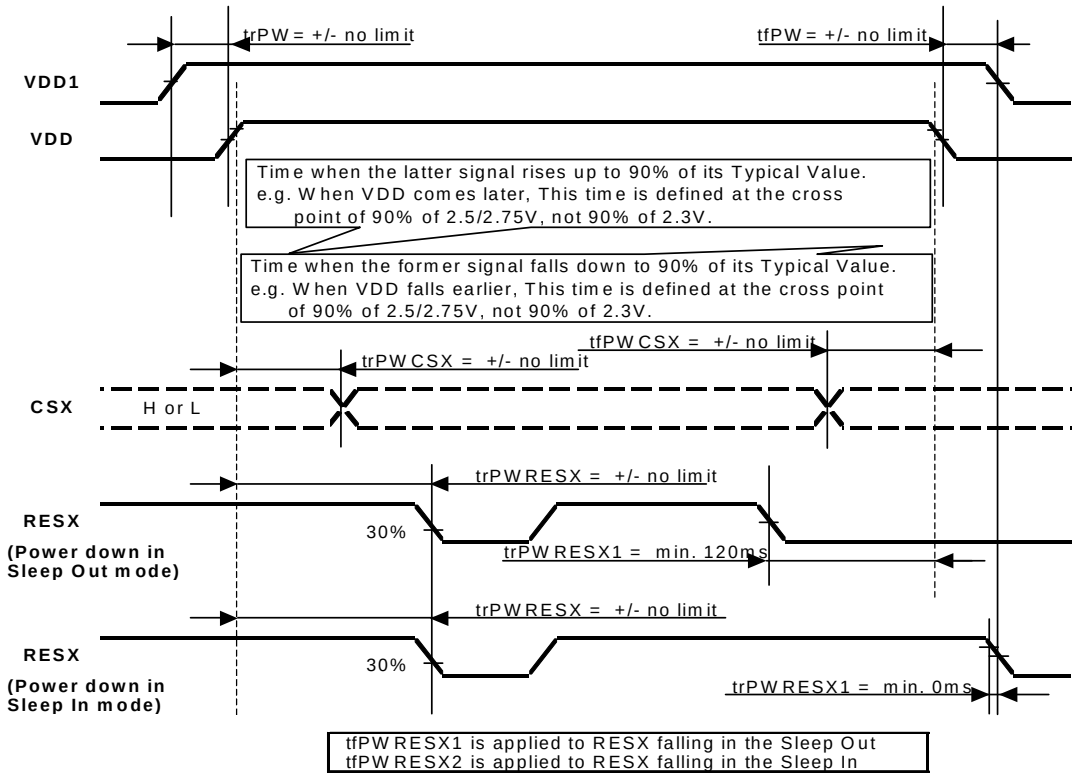
VDDI and VDD can be applied in any order.
VDD and VDDI can be powered down in any order.
During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.
During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Notes:
1. There will be no damage to the display module if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
4. If RESX line is not held stable by host during Power On Sequence as defined in Sections 8.5.1 and 8.5.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

8.5.1. Case 1 – RESX line is held High or Unstable by Host at Power On

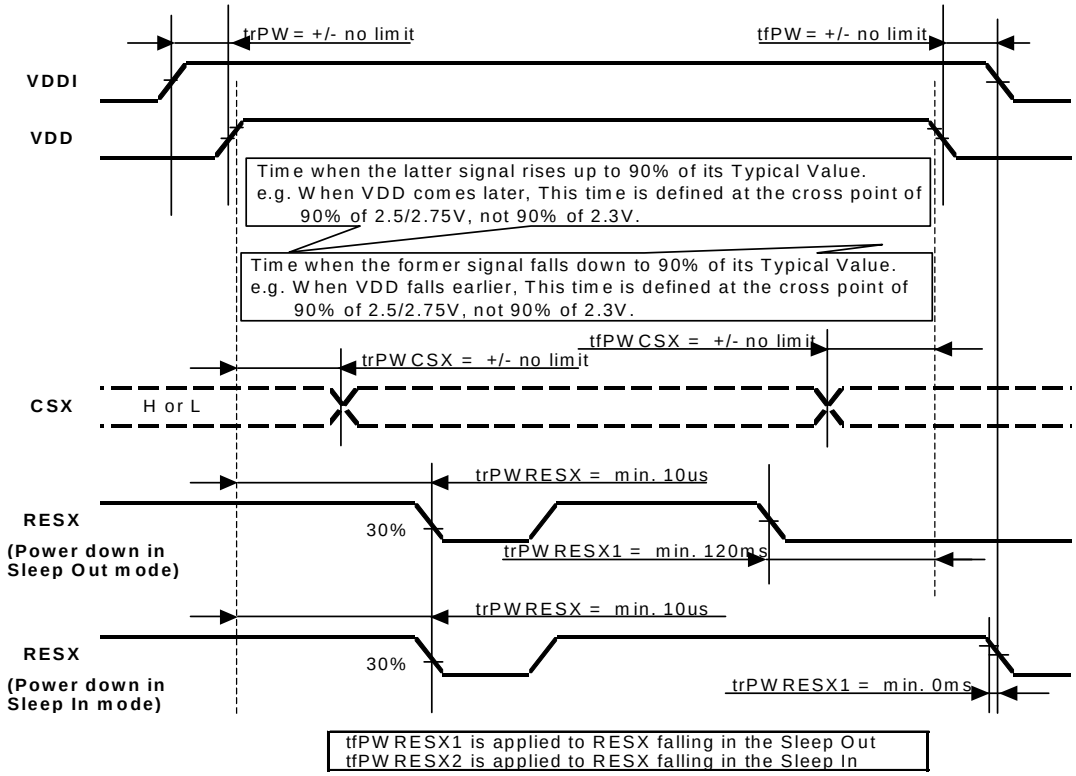
If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

8.5.2. Case 2 – RESX line is held Low by host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10usec after both VDD and VDDI have been applied.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

8.5.3. Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. The display module must meet following requirements:

1. There cannot be any damages for the display module or the display module cannot cause any damages for the host or lines of the interface.
2. There cannot be any abnormal visible effects (= display must be blank) with in 1 second on the display and remains blank until “Power On Sequence” powers it up.

8.6. Power Level Definition

8.6.1. Power levels

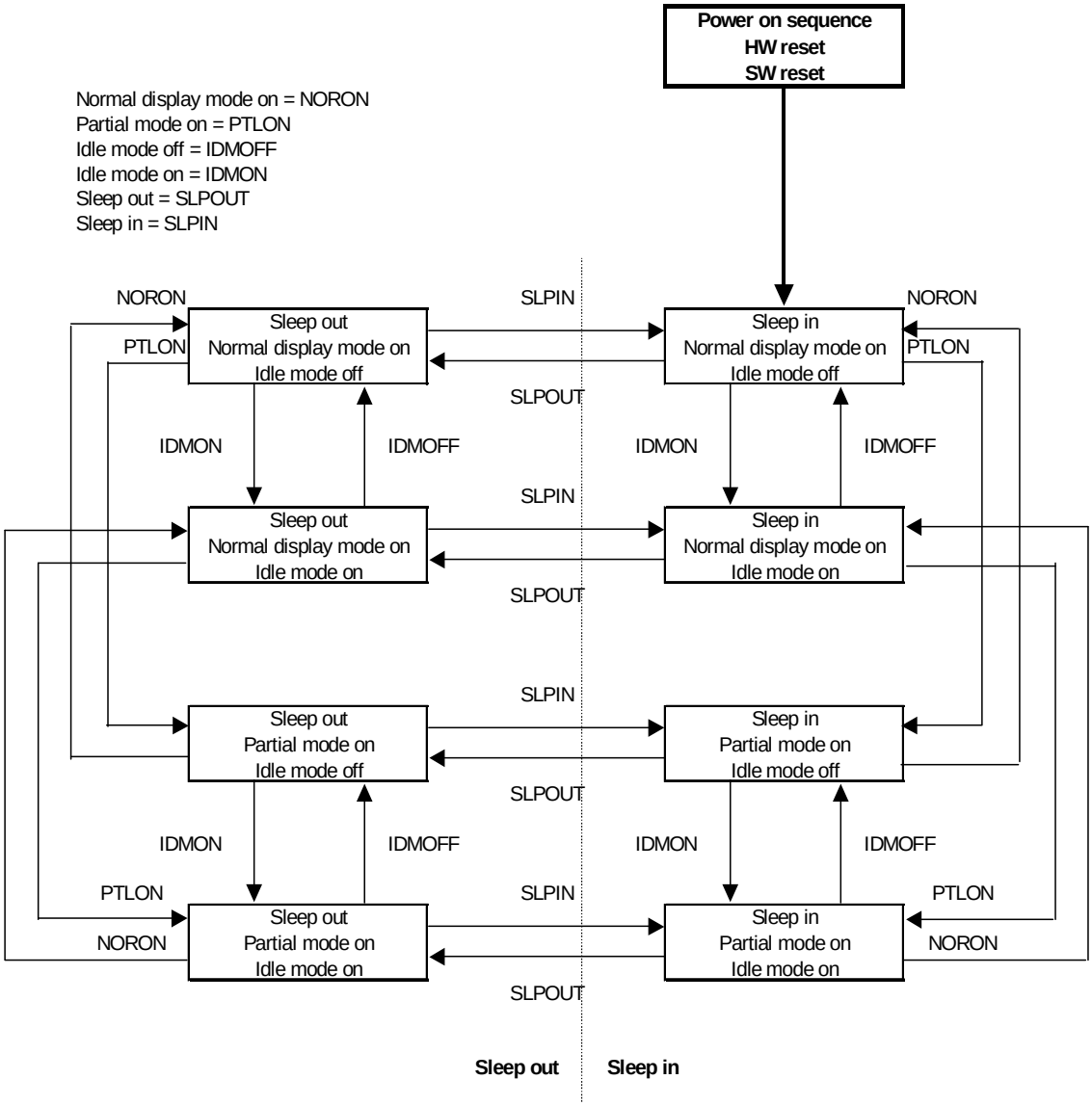
6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 16,777,216 colours.
2. Partial Mode On, Idle Mode Off, Sleep Out.
   In this mode part of the display is used with maximum 16,777,216 colours.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display area is used but with 8 colours.
4. Partial Mode On, Idle Mode On, Sleep Out.
   In this mode, part of the display is used but with 8 colours.
5. Sleep In Mode.
   In this mode, the DC:DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.
6. Power Off Mode.

In this mode, both VDD and VDDI are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

8.6.2. Power flow chart



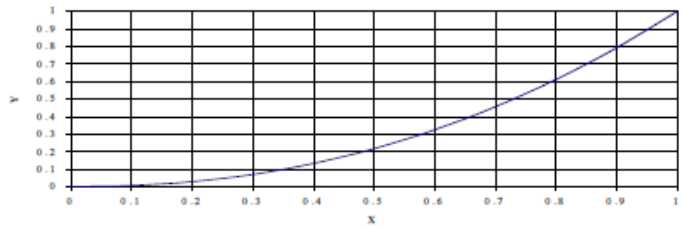
Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.
Note 2: There is not any limitation, which is not specified by final customer, when there is changing from one power mode to another power mode.

8.7 Gamma Curves

MC2PA8201 incorporates a gamma adjustment.
We show γ characteristic to recommend as follows.

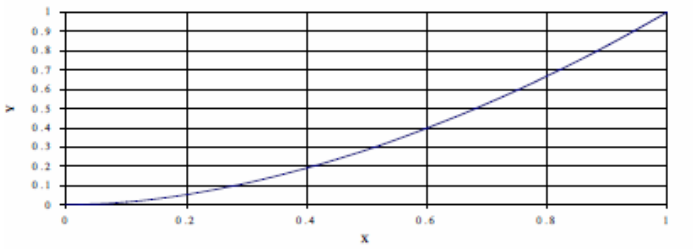
8.7.1. Gamma Curve 1 (GC0), applies the function y=x2.2

Gamma $y = x^{2.2}$



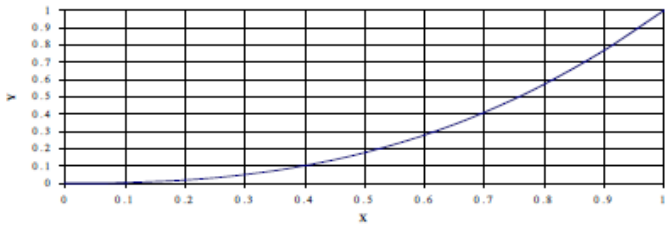
8.7.2. Gamma Curve 2 (GC1), applies the function y=x1.8

Gamma $y = x^{1.8}$



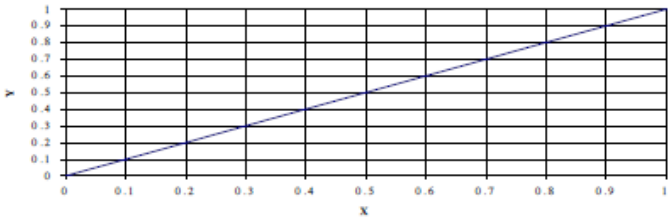
8.7.3. Gamma Curve 3 (GC2), applies the function y=x2.5

Gamma $y = x^{2.5}$



8.7.4. Gamma Curve 4 (GC3) is linear, i.e. y=x1

Gamma $y = x^{1}$


y
x
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1

8.8. Reset

8.8.1. Registers

The registers that are initialised are listed below.

	After Powered On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep	In	In	In
Display mode	Normal	Normal	Normal
Inversion	Off	Off	Off
Display	Off	Off	Off
Idle	Off	Off	Off
Column Start Address	0000h	0000h	0000h
Column End Address	00EFh	00EFh	if MADCTL's B5 =0: 00EFh if MADCTL's B5 =1: 013Fh
Page Start Address	0000h	0000h	0000h
Page End Address	013Fh	013Fh	if MADCTL's B5 =0: 013Fh if MADCTL's B5 =1: 00EFh
Colour Set R[18:0][7:0] G[18:0][7:0] B[18:0][7:0]	Random	No Change	No Change
Gamma setting	GC0	GC0	GC0
Partial Area start	0000h	0000h	0000h
Partial Area end	013Fh	013Fh	013Fh
Vertical scroll Top fixed area	0000h	0000h	0000h
Vertical scroll area	0140h	0140h	0140h
Vertical scroll Bottom fixed area	0000h	0000h	0000h
Vertical scroll Start address	0000h	0000h	0000h
Colour Pixel Format	24 Bit/Pixel	24 Bit/Pixel	No Change
Memory Data Access Control	00h	00h	No Change
Vertical Scrolling	Off	Off	Off
RDDPM	08h	08h	08h
RDDMADCTL	00h	00h	No Change
RDDCOLMOD	24 Bit/Pixel	24 Bit/Pixel	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
TE Output Line Off	Off	Off	Off
TE Line Mode	Mode 1 (3)	Mode 1 (3)	Mode 1 (3)

Notes:
1. There will be no abnormal visible effects on the display when S/W or H/W Resets are applied.
2. Powered-On Reset finishes within 10µs after both VDD & VDDI are applied.
3. Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

8.8.2. Module Input/Output Pins

8.8.2.1. Output Pins, I/O Pins

	After Powered On	After Hardware Reset	After Software Reset
TE Line	Low	Low	Low
D[15...0] (output driver)	High Z(Inactive)	High Z(Inactive)	High Z(Inactive)

Note: There will be no output from D[15...0] during Power On/Off sequences, Hardware Reset and Software Reset.

8.8.2.2. Input pins

	During Power On Process	After Powered On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	See 8.5	Input valid	Input valid	Input valid	See 8.5
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D[15…0] (input driver)	Input invalid	Input valid	Input valid	Input valid	Input invalid

8.8.3. Reset Timing

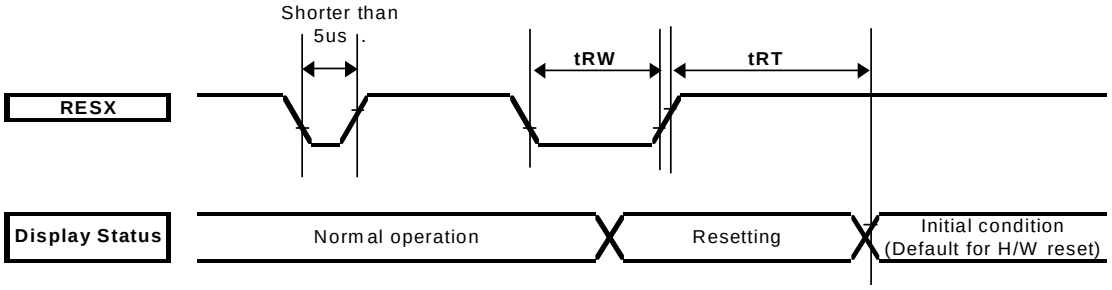


Table 8.9.3 Reset timing

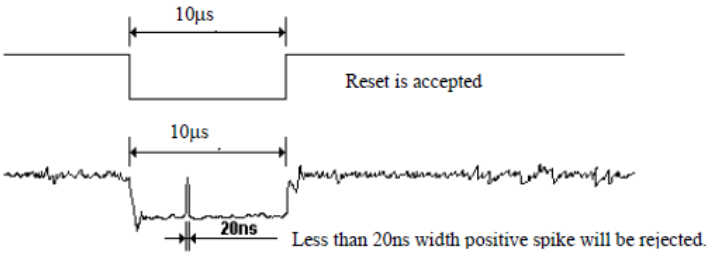
Signal	Symbol	Parameter	Min.	Max.	Unit
RESX	tRW	Reset pulse duration	10		us
	tRT	Reset cancel		5 (note 5)	ms
				120 (notes 6, 7)	ms

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than ~5us	Reset Rejected
Longer than 9us	Reset
Between ~5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8.9. Colour depth conversion look up table - 4,096, 65,536 and 262,144 *colours to 16,777,216 colour*

R input (4bit) 12 bit/pixel - mode 4,096 colours	R input (5 bit) 16 bit/pixel - mode 65,536 colours	R input (6 bit) 18 bit/pixel mode 262,144 colours	R output (8bit) 24 bit/pixel -mode 16,777,216 colours	RGBSET Parameter
0000	00000	000000	R007 R006 R005 R004 R003 R002 R001 R000	1
0001	00001	000001	R017 R016 R015 R014 R013 R012 R011 R010	2
0010	00010	000010	R027 R026 R025 R024 R023 R022 R021 R020	3
0011	00011	000011	R037 R036 R035 R034 R033 R032 R031 R030	4
0100	00100	000100	R047 R046 R045 R044 R043 R042 R041 R040	5
0101	00101	000101	R057 R056 R055 R054 R053 R052 R051 R050	6
0110	00110	000110	R067 R066 R065 R064 R063 R062 R061 R060	7
0111	00111	000111	R077 R076 R075 R074 R073 R072 R071 R070	8
1000	01000	001000	R087 R086 R085 R084 R083 R082 R081 R080	9
1001	01001	001001	R097 R096 R095 R094 R093 R092 R091 R090	10
1010	01010	001010	R107 R106 R105 R104 R103 R102 R101 R100	11
1011	01011	001011	R117 R116 R115 R114 R113 R112 R111 R110	12
1100	01100	001100	R127 R126 R125 R124 R123 R122 R121 R120	13
1101	01101	001101	R137 R136 R135 R134 R133 R132 R131 R130	14
1110	01110	001110	R147 R146 R145 R144 R143 R142 R141 R140	15
1111	01111	001111	R157 R156 R155 R154 R153 R152 R151 R150	16
No Input	10000	010000	R167 R166 R165 R164 R163 R162 R161 R160	17
No Input	10001	010001	R177 R176 R175 R174 R173 R172 R171 R170	18
No Input	10010	010010	R187 R186 R185 R184 R183 R182 R181 R180	19
No Input	10011	010011	R197 R196 R195 R194 R193 R192 R191 R190	20
No Input	10100	010100	R207 R206 R205 R204 R203 R202 R201 R200	21
No Input	10101	010101	R217 R216 R215 R214 R213 R212 R211 R210	22
No Input	10110	010110	R227 R226 R225 R224 R223 R222 R221 R220	23
No Input	10111	010111	R237 R236 R235 R234 R233 R232 R231 R230	24
No Input	11000	011000	R247 R246 R245 R244 R243 R242 R241 R240	25
No Input	11001	011001	R257 R256 R255 R254 R253 R252 R251 R250	26
No Input	11010	011010	R267 R266 R265 R264 R263 R262 R261 R260	27
No Input	11011	011011	R277 R276 R275 R274 R273 R272 R271 R270	28
No Input	11100	011100	R287 R286 R285 R284 R283 R282 R281 R280	29
No Input	11101	011101	R297 R296 R295 R294 R293 R292 R291 R290	30
No Input	11110	011110	R307 R306 R305 R304 R303 R302 R301 R300	31
No Input	11111	011111	R317 R316 R315 R314 R313 R312 R311 R310	32

R input (4bit) 12 bit/pixel - mode 4,096 colours	R input (5 bit) 16 bit/pixel - mode 65,536 colours	R input (6 bit) 18 bit/pixel mode 262,144 colours	R output (8bit) 24 bit/pixel -mode 16,777,216 colours	RGBSET Parameter
No Input	No Input	100000	R327 R326 R325 R324 R323 R322 R321 R320	33
No Input	No Input	100001	R337 R336 R335 R334 R333 R332 R331 R330	34
No Input	No Input	100010	R347 R346 R345 R344 R343 R342 R341 R340	35
No Input	No Input	100011	R357 R356 R355 R354 R353 R352 R351 R350	36
No Input	No Input	100100	R367 R366 R365 R364 R363 R362 R361 R360	37
No Input	No Input	100101	R377 R376 R375 R374 R373 R372 R371 R370	38
No Input	No Input	100110	R387 R386 R385 R384 R383 R382 R381 R380	39
No Input	No Input	100111	R397 R396 R395 R394 R393 R392 R391 R390	40
No Input	No Input	101000	R407 R406 R405 R404 R403 R402 R401 R400	41
No Input	No Input	101001	R417 R416 R415 R414 R413 R412 R411 R410	42
No Input	No Input	101010	R427 R426 R425 R424 R423 R422 R421 R420	43
No Input	No Input	101011	R437 R436 R435 R434 R433 R432 R431 R430	44
No Input	No Input	101100	R447 R446 R445 R444 R443 R442 R441 R440	45
No Input	No Input	101101	R457 R456 R455 R454 R453 R452 R451 R450	46
No Input	No Input	101110	R467 R466 R465 R464 R463 R462 R461 R460	47
No Input	No Input	101111	R477 R476 R475 R474 R473 R472 R471 R470	48
No Input	No Input	110000	R487 R486 R485 R484 R483 R482 R481 R480	49
No Input	No Input	110001	R497 R496 R495 R494 R493 R492 R491 R490	50
No Input	No Input	110010	R507 R506 R505 R504 R503 R502 R501 R500	51
No Input	No Input	110011	R517 R516 R515 R514 R513 R512 R511 R510	52
No Input	No Input	110100	R527 R526 R525 R524 R523 R522 R521 R520	53
No Input	No Input	110101	R537 R536 R535 R534 R533 R532 R531 R530	54
No Input	No Input	110110	R547 R546 R545 R544 R543 R542 R541 R540	55
No Input	No Input	110111	R557 R556 R555 R554 R553 R552 R551 R550	56
No Input	No Input	111000	R567 R566 R565 R564 R563 R562 R561 R560	57
No Input	No Input	111001	R577 R576 R575 R574 R573 R572 R571 R570	58
No Input	No Input	111010	R587 R586 R585 R584 R583 R582 R581 R580	59
No Input	No Input	111011	R597 R596 R595 R594 R593 R592 R591 R590	60
No Input	No Input	111100	R607 R606 R605 R604 R603 R602 R601 R600	61
No Input	No Input	111101	R617 R616 R615 R614 R613 R612 R611 R610	62
No Input	No Input	111110	R627 R626 R625 R624 R623 R622 R621 R620	63
No Input	No Input	111111	R637 R636 R635 R634 R633 R632 R631 R630	64

G input (4bit) 12 bit/pixel - mode 4,096 colours	G input (6 bit) 16 bit/pixel - mode 65,536 colours	G input (6 bit) 18 bit/pixel - mode 262,144 colours	G output (8bit) 24 bit/pixel -mode 16,777,216 colours	RGBSET Parameter
0000	000000	000000	G007 G006 G005 G004 G003 G002 G001 G000	65
0001	000001	000001	G017 G016 G015 G014 G013 G012 G011 G010	66
0010	000010	000010	G027 G026 G025 G024 G023 G022 G021 G020	67
0011	000011	000011	G037 G036 G035 G034 G033 G032 G031 G030	68
0100	000100	000100	G047 G046 G045 G044 G043 G042 G041 G040	69
0101	000101	000101	G057 G056 G055 G054 G053 G052 G051 G050	70
0110	000110	000110	G067 G066 G065 G064 G063 G062 G061 G060	71
0111	000111	000111	G077 G076 G075 G074 G073 G072 G071 G070	72
1000	001000	001000	G087 G086 G085 G084 G083 G082 G081 G080	73
1001	001001	001001	G097 G096 G095 G094 G093 G092 G091 G090	74
1010	001010	001010	G107 G106 G105 G104 G103 G102 G101 G100	75
1011	001011	001011	G117 G116 G115 G114 G113 G112 G111 G110	76
1100	001100	001100	G127 G126 G125 G124 G123 G122 G121 G120	77
1101	001101	001101	G137 G136 G135 G134 G133 G132 G131 G130	78
1110	001110	001110	G147 G146 G145 G144 G143 G142 G141 G140	79
1111	001111	001111	G157 G156 G155 G154 G153 G152 G151 G150	80
No Input	010000	010000	G167 G166 G165 G164 G163 G162 G161 G160	81
No Input	010001	010001	G177 G176 G175 G174 G173 G172 G171 G170	82
No Input	010010	010010	G187 G186 G185 G184 G183 G182 G181 G180	83
No Input	010011	010011	G197 G196 G195 G194 G193 G192 G191 G190	84
No Input	010100	010100	G207 G206 G205 G204 G203 G202 G201 G200	85
No Input	010101	010101	G217 G216 G215 G214 G213 G212 G211 G210	86
No Input	010110	010110	G227 G226 G225 G224 G223 G222 G221 G220	87
No Input	010111	010111	G237 G236 G235 G234 G233 G232 G231 G230	88
No Input	011000	011000	G247 G246 G245 G244 G243 G242 G241 G240	89
No Input	011001	011001	G257 G256 G255 G254 G253 G252 G251 G250	90
No Input	011010	011010	G267 G266 G265 G264 G263 G262 G261 G260	91
No Input	011011	011011	G277 G276 G275 G274 G273 G272 G271 G270	92
No Input	011100	011100	G287 G286 G285 G284 G283 G282 G281 G280	93
No Input	011101	011101	G297 G296 G295 G294 G293 G292 G291 G290	94
No Input	011110	011110	G307 G306 G305 G304 G303 G302 G301 G300	95
No Input	011111	011111	G317 G316 G315 G314 G313 G312 G311 G310	96

G input (4bit) 12 bit/pixel - mode 4,096 colours	G input (6 bit) 16 bit/pixel - mode 65,536 colours	G input (6 bit) 18 bit/pixel - mode 262,144 colours	G output (8bit) 24 bit/pixel -mode 16,777,216 colours	RGBSET Parameter
No Input	100000	100000	G327 G326 G325 G324 G323 G322 G321 G320	97
No Input	100001	100001	G337 G336 G335 G334 G333 G332 G331 G330	98
No Input	100010	100010	G347 G346 G345 G344 G343 G342 G341 G340	99
No Input	100011	100011	G357 G356 G355 G354 G353 G352 G351 G350	100
No Input	100100	100100	G367 G366 G365 G364 G363 G362 G361 G360	101
No Input	100101	100101	G377 G376 G375 G374 G373 G372 G371 G370	102
No Input	100110	100110	G387 G386 G385 G384 G383 G382 G381 G380	103
No Input	100111	100111	G397 G396 G395 G394 G393 G392 G391 G390	104
No Input	101000	101000	G407 G406 G405 G404 G403 G402 G401 G400	105
No Input	101001	101001	G417 G416 G415 G414 G413 G412 G411 G410	106
No Input	101010	101010	G427 G426 G425 G424 G423 G422 G421 G420	107
No Input	101011	101011	G437 G436 G435 G434 G433 G432 G431 G430	108
No Input	101100	101100	G447 G446 G445 G444 G443 G442 G441 G440	109
No Input	101101	101101	G457 G456 G455 G454 G453 G452 G451 G450	110
No Input	101110	101110	G467 G466 G465 G464 G463 G462 G461 G460	111
No Input	101111	101111	G477 G476 G475 G474 G473 G472 G471 G470	112
No Input	110000	110000	G487 G486 G485 G484 G483 G482 G481 G480	113
No Input	110001	110001	G497 G496 G495 G494 G493 G492 G491 G490	114
No Input	110010	110010	G507 G506 G505 G504 G503 G502 G501 G500	115
No Input	110011	110011	G517 G516 G515 G514 G513 G512 G511 G510	116
No Input	110100	110100	G527 G526 G525 G524 G523 G522 G521 G520	117
No Input	110101	110101	G537 G536 G535 G534 G533 G532 G531 G530	118
No Input	110110	110110	G547 G546 G545 G544 G543 G542 G541 G540	119
No Input	110111	110111	G557 G556 G555 G554 G553 G552 G551 G550	120
No Input	111000	111000	G567 G566 G565 G564 G563 G562 G561 G560	121
No Input	111001	111001	G577 G576 G575 G574 G573 G572 G571 G570	122
No Input	111010	111010	G587 G586 G585 G584 G583 G582 G581 G580	123
No Input	111011	111011	G597 G596 G595 G594 G593 G592 G591 G590	124
No Input	111100	111100	G607 G606 G605 G604 G603 G602 G601 G600	125
No Input	111101	111101	G617 G616 G615 G614 G613 G612 G611 G610	126
No Input	111110	111110	G627 G626 G625 G624 G623 G622 G621 G620	127
No Input	111111	111111	G637 G636 G635 G634 G633 G632 G631 G630	128

B input (4bit) 12 bit/pixel - mode 4,096 colours	B input (5 bit) 16 bit/pixel - mode 65,536 colours	B input (6 bit) 18 bit/pixel - mode 262,144 colours	B output (8bit) 24 bit/pixel -mode 16,777,216 colours	RGBSET Parameter
0000	00000	000000	B007 B006 B005 B004 B003 B002 B001 B000	129
0001	00001	000001	B017 B016 B015 B014 B013 B012 B011 B010	130
0010	00010	000010	B027 B026 B025 B024 B023 B022 B021 B020	131
0011	00011	000011	B037 B036 B035 B034 B033 B032 B031 B030	132
0100	00100	000100	B047 B046 B045 B044 B043 B042 B041 B040	133
0101	00101	000101	B057 B056 B055 B054 B053 B052 B051 B050	134
0110	00110	000110	B067 B066 B065 B064 B063 B062 B061 B060	135
0111	00111	000111	B077 B076 B075 B074 B073 B072 B071 B070	136
1000	01000	001000	B087 B086 B085 B084 B083 B082 B081 B080	137
1001	01001	001001	B097 B096 B095 B094 B093 B092 B091 B090	138
1010	01010	001010	B107 B106 B105 B104 B103 B102 B101 B100	139
1011	01011	001011	B117 B116 B115 B114 B113 B112 B111 B110	140
1100	01100	001100	B127 B126 B125 B124 B123 B122 B121 B120	141
1101	01101	001101	B137 B136 B135 B134 B133 B132 B131 B130	142
1110	01110	001110	B147 B146 B145 B144 B143 B142 B141 B140	143
1111	01111	001111	B157 B156 B155 B154 B153 B152 B151 B150	144
No Input	10000	010000	B167 B166 B165 B164 B163 B162 B161 B160	145
No Input	10001	010001	B177 B176 B175 B174 B173 B172 B171 B170	146
No Input	10010	010010	B187 B186 B185 B184 B183 B182 B181 B180	147
No Input	10011	010011	B197 B196 B195 B194 B193 B192 B191 B190	148
No Input	10100	010100	B207 B206 B205 B204 B203 B202 B201 B200	149
No Input	10101	010101	B217 B216 B215 B214 B213 B212 B211 B210	150
No Input	10110	010110	B227 B226 B225 B224 B223 B222 B221 B220	151
No Input	10111	010111	B237 B236 B235 B234 B233 B232 B231 B230	152
No Input	11000	011000	B247 B246 B245 B244 B243 B242 B241 B240	153
No Input	11001	011001	B257 B256 B255 B254 B253 B252 B251 B250	154
No Input	11010	011010	B267 B266 B265 B264 B263 B262 B261 B260	155
No Input	11011	011011	B277 B276 B275 B274 B273 B272 B271 B270	156
No Input	11100	011100	B287 B286 B285 B284 B283 B282 B281 B280	157
No Input	11101	011101	B297 B296 B295 B294 B293 B292 B291 B290	158
No Input	11110	011110	B307 B306 B305 B304 B303 B302 B301 B300	159
No Input	11111	011111	B317 B316 B315 B314 B313 B312 B311 B310	160

B input (4bit) 12 bit/pixel - mode 4,096 colours	B input (5 bit) 16 bit/pixel - mode 65,536 colours	B input (6 bit) 18 bit/pixel - mode 262,144 colours	B output (8bit) 24 bit/pixel -mode 16,777,216 colours	RGBSET Parameter
No Input	No Input	100000	B327 B326 B325 B324 B323 B322 B321 B320	161
No Input	No Input	100001	B337 B336 B335 B334 B333 B332 B331 B330	162
No Input	No Input	100010	B347 B346 B345 B344 B343 B342 B341 B340	163
No Input	No Input	100011	B357 B356 B355 B354 B353 B352 B351 B350	164
No Input	No Input	100100	B367 B366 B365 B364 B363 B362 B361 B360	165
No Input	No Input	100101	B377 B376 B375 B374 B373 B372 B371 B370	166
No Input	No Input	100110	B387 B386 B385 B384 B383 B382 B381 B380	167
No Input	No Input	100111	B397 B396 B395 B394 B393 B392 B391 B390	168
No Input	No Input	101000	B407 B406 B405 B404 B403 B402 B401 B400	169
No Input	No Input	101001	B417 B416 B415 B414 B413 B412 B411 B410	170
No Input	No Input	101010	B427 B426 B425 B424 B423 B422 B421 B420	171
No Input	No Input	101011	B437 B436 B435 B434 B433 B432 B431 B430	172
No Input	No Input	101100	B447 B446 B445 B444 B443 B442 B441 B440	173
No Input	No Input	101101	B457 B456 B455 B454 B453 B452 B451 B450	174
No Input	No Input	101110	B467 B466 B465 B464 B463 B462 B461 B460	175
No Input	No Input	101111	B477 B476 B475 B474 B473 B472 B471 B470	176
No Input	No Input	110000	B487 B486 B485 B484 B483 B482 B481 B480	177
No Input	No Input	110001	B497 B496 B495 B494 B493 B492 B491 B490	178
No Input	No Input	110010	B507 B506 B505 B504 B503 B502 B501 B500	179
No Input	No Input	110011	B517 B516 B515 B514 B513 B512 B511 B510	180
No Input	No Input	110100	B527 B526 B525 B524 B523 B522 B521 B520	181
No Input	No Input	110101	B537 B536 B535 B534 B533 B532 B531 B530	182
No Input	No Input	110110	B547 B546 B545 B544 B543 B542 B541 B540	183
No Input	No Input	110111	B557 B556 B555 B554 B553 B552 B551 B550	184
No Input	No Input	111000	B567 B566 B565 B564 B563 B562 B561 B560	185
No Input	No Input	111001	B577 B576 B575 B574 B573 B572 B571 B570	186
No Input	No Input	111010	B587 B586 B585 B584 B583 B582 B581 B580	187
No Input	No Input	111011	B597 B596 B595 B594 B593 B592 B591 B590	188
No Input	No Input	111100	B607 B606 B605 B604 B603 B602 B601 B600	189
No Input	No Input	111101	B617 B616 B615 B614 B613 B612 B611 B610	190
No Input	No Input	111110	B627 B626 B625 B624 B623 B622 B621 B620	191
No Input	No Input	111111	B637 B636 B635 B634 B633 B632 B631 B630	192

9. Absolute Maximum Ratings

Table9.-1

Item	Symbol	Unit	Value	Notes
Power supply voltage(1)	VCCI-GND	V	-0.3 to 2.2	1,3
Power supply voltage(2)	VCC-GND	V	-0.3 to 4.6	1,2
Power supply voltage(3)	VCCA-GND	V	-0.3 to 4.6	1,2
Power supply voltage(4)	VOUT1-GND	V	-0.3 to 6.3	1,4
Power supply voltage(5)	VREG-GND	V	-0.3 to 6.3	1,5
Power supply voltage(6)	VGH-GND	V	-0.3 to 16.5	1,6
Power supply voltage(7)	GND-VGL	V	-0.3 to 16.5	1,7
Power supply voltage(8)	VGH-VGL	V	<32	1,6,7,8
Power supply voltage(9)	GND-VCL	V	-0.3 to 4.6	1
Input signal voltage	Vt	V	-0.3 to VCCI+0.3	1
Operation temperature	Topr	Degrees C	-40 to+85	1
Storage temperature	Tstg	Degrees C	-55 to+110	1

Note 1) If used beyond the absolute maximum ratings, the LSI may be permanently damaged. It is strongly recommended to use the LSI at a condition within the electrical characteristics for normal operation. Exposure to a condition not within the electrical characteristics may affect device's reliability.

Note 2) Make sure: VCC = VCCA $\geq$ GND.

Note 3) Make sure: VCCI $\geq$ GND.

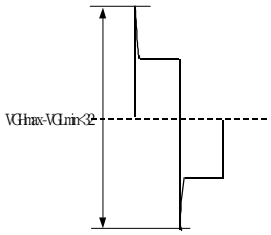
Note 4) Make sure: VOUT1 $\geq$ GND.

Note 5) Make sure: VOUT1-0.3V $\geq$ VREG.

Note 6) Make sure: VGH $\geq$ GND.

Note 7) Make sure: GND $\geq$ VGL.

Note 8) Not over than absolute maximum voltage including the panel in On/Off and the ripple voltage of wave pattern.



10. Electric Characteristics

10.1. DC Characteristics(VCC=2.60V to 2.95V,Ta=-40 to +85 degree C)

Item		Symbol	Unit	Test Condition	Min.	Typ.	Max.
Input high voltage		VIH	V	VCCI=1.65V to 1.95V	0.7 x VCCI	-	VCCI
Input low voltage		VIL	V	VCCI=1.65V to 1.95V	-0.3	-	0.3 x VCCI
Output high voltage (DB15-DB0)		VOH1	V	VCCI=1.65V to 1.95V, IOH=-0.1mA	0.8 x VCCI	-	-
Output low voltage (DB15- DB0)		VOL1	V	VCCI=1.65V to 1.95V, IOL=0.1mA	-	-	0.2 x VCCI
I/O leakage current		ILi	uA	Vin=0 to VCCI	-1	-	1
Current consumption (VCC, VCCI -GND)	Normal display mode	IOP1	mA	Ta=25 degrees C, VCCI=1.8V, VCC=2.8 V Frame reverse RC Oscillation: fosc=920kHz Frame frequency=61Hz 1H clocks=46,FP=BP=4 VR1=3.76V,VR2=2.42V(expected value) fcp1=fcp3=10KHz,fcp2=5KHz Teester Load (~100pF)	5.31	6.63	7.95
Current consumption (VCC, VCCI -GND)	8-color/ partial display mode	IOP2	mA	Ta=25 degrees C, 8-color display, VCC, VCCA=2.8V,VCCI=1.8V Frame reverse RC Oscillation: fosc=920kHz	0.80	1.00	1.20
Current consumption (VCC, VCCI-GND)	Sleep mode	IST	uA	VCC, VCCA=2.8V, VCCI=1.8V, Ta=25 degrees C	-	'-	10.0

Table10.1.- 1

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.
Step-up output voltage	VOUT1	V	VCC=VCCA= 2.8V,VCCI=1.8V, fosc=920kHz, Ta=25 degrees C. VR1=[1000]=3.762V, VR2=[1000]=2.420, C11=C12=C21=C22=C13=1uF/B characteristics VOUT1=VGH=VGL=VCL=1uF/B characteristics No panel load, Iload=1.5mA	4.95	'-	5.60
	VREG	V	VCC=VCCA= 2.8V,VCCI=1.8V, fosc=920kHz, Ta=25 degrees C. VR1=[1000]=3.762V, VR2=[1000]=2.420, VREG=[01000]=4.000, C11=C12=C21=C22=C13=1uF/B characteristics VOUT1=VGH=VGL=VCL=1uF/B characteristics No panel load,	3.00	'-	4.12
	VGH	V	VCC=VCCA=2.8VV,VCCI=1.8V fosc=920kHz, Ta=25 degrees C. VR1=[1000]=3.762V, VR2=[1000]=2.420, VGH=2xVR1+VR2 C11=C12=C21=C22=C13=1uF/B characteristics VOUT1=VGH=VGL=VCL=1uF/B characteristics No panel load, Iload=-100uA	9.00	-	9.85
	VGL	V	VCC=VCCA=2.75V,VCCI=!.8V fosc=920kHz, Ta=25 degrees C. VR1=[1000]=3.762V, VR2=[1000]=2.420 VGL=-1x(VR1+VR2), C11=C12=C21=C22=C13=1uF/B characteristics VOUT1=VGH=VGL=VCL=1uF/B characteristics No panel load, Iload=+100uA	-6.00	-	-5.40
	VGH-VGL	V	Please use even a mode to be at the time of movement within max value.	-	-	(27.5)
	VCL	V	VCC=VCCA=2.8V,VCCI=1.8V fosc=920KHz, Ta=25 degrees C. VCL=-1xVCC C11=C12=C21=C22=C13=1uF/B characteristics VOUT1=VGH=VGL=VCL=1uF/B characteristics No panel load, Iload=+500uA	2.30	'-	2.80-

Table10.1-2

10.2. AC Characteristics

8,16bit bus interface operation

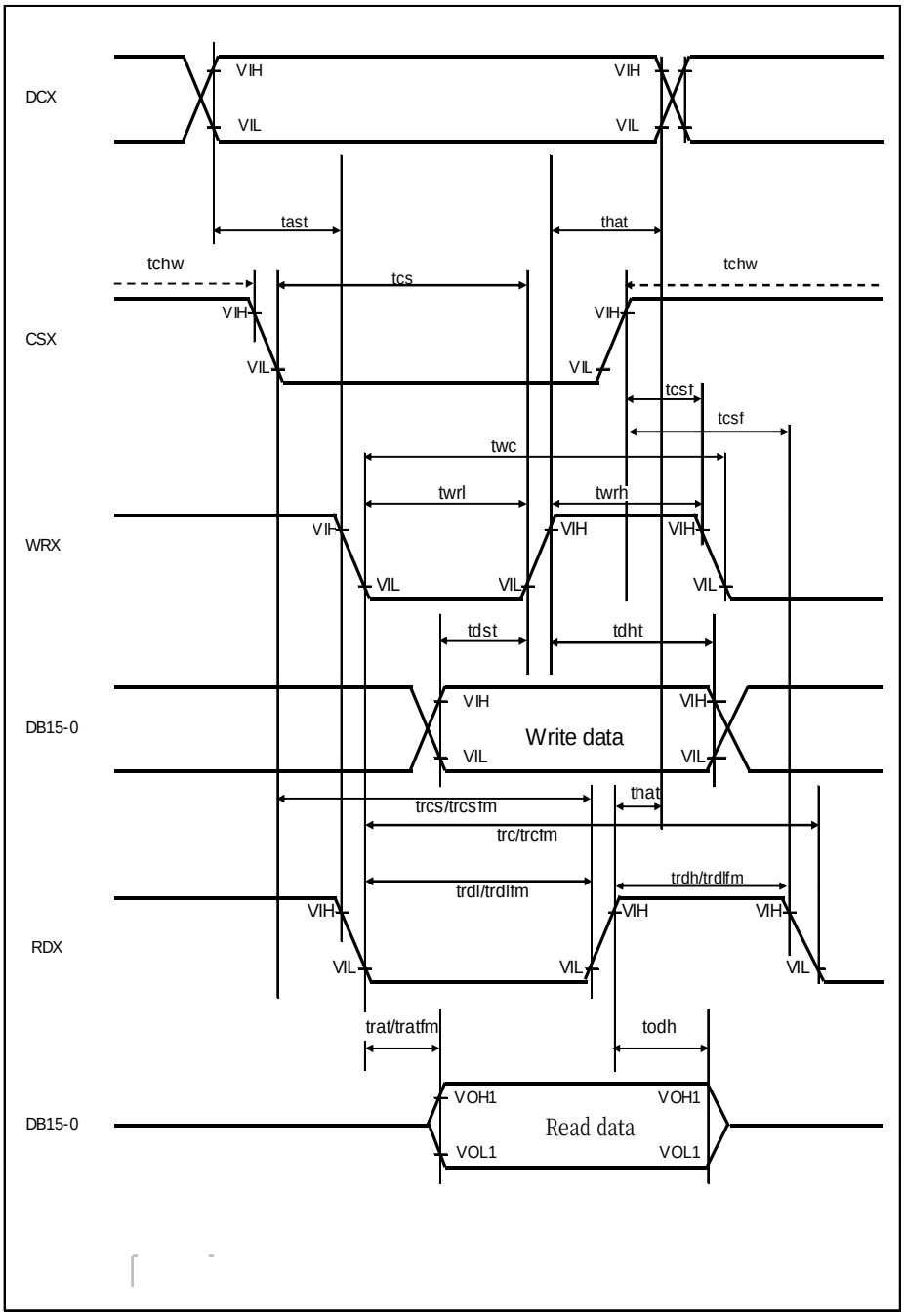


Fig 10.2.-1

Reset operation

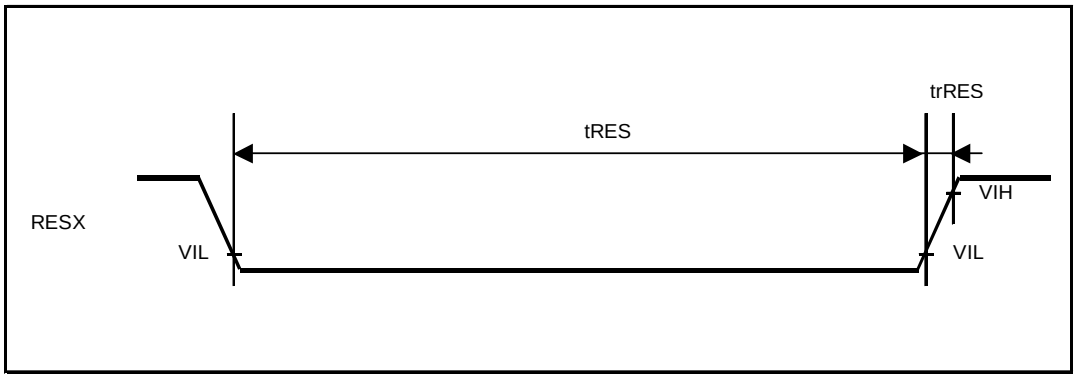


Fig 10.2.-2

Table 10.2.-1: Clock Characteristics

Item	Symbol	Unit	Timing diagram	Min	Typ	Max
RC Oscillation clock	tosc	kHz	VCC=2.8, VCCI=1.8V	892.4	920.0	947.6

fosc=fTEx1Hclocksx(320+BP+FP) fTE: frame frequency,BP=2H, FP=2H, lHclocks=46

Table 10.2.-2: MeSSI mode(16-/8-bit mode), VCC=2.6 to 2.95V, VCCI=1.65V to 1.95V

Item	Symbol	Unit	Timing diagram	Min	Typ	Max
Address setup time	tast	ns	Figure 11.2.-1	10	-	-
Address hold time	taht	ns	Figure 11.2.-1	10	-	
CSX “H” pulse width	tchw	ns	Figure 11.2.-1	0	-	-
Chip select setup time (write)	tcs	ns	Figure 11.2.-1	35	-	-
Chip select setup time (Read)	trcs	ns	Figure 11.2.-1	45	-	-
Chip select setup time (Read FM)	trcsfm	ns	Figure 11.2.-1	355	-	-
Chip select wait time (Write/Read)	tcsf	ns	Figure 11.2.-1	10	-	-
Write cycle	twc	ns	Figure 11.2.-1	100	-	-
Control pulse “H” duration	twrh	ns	Figure 11.2.-1	35	-	-
Control pulse “L” duration	twrl	ns	Figure 11.2.-1	35	-	-
Read cycle (ID)	trc	ns	Figure 11.2.-1	160	-	-
Read cycle (FM)	trcfm	ns	Figure 11.2.-1	450	-	-
Control pulse “H” duration (ID)	trdh	ns	Figure 11.2.-1	90	-	-
Control pulse “L” duration (ID)	trdl	ns	Figure 11.2.-1	45	-	-
Control pulse “H” duration (FM)	trdhfm	ns	Figure 11.2.-1	90	-	-
Control pulse “L” duration (FM)	trdlfm	ns	Figure 11.2.-1	355	-	-
Data setup time	tdst	ns	Figure 11.2.-1	10	-	-
Data hold time	tdht	ns	Figure 11.2.-1	10	-	-
Read access time (ID)	trat	ns	Figure 11.2.-1	-		40
Read access time(FM)	tratfm	ns	Figure 11.2.-1	-		340
Output disable time	todh	ns	Figure 11.2.-1	20		80

Table 10.2.-3 Reset operation

Item	Symbol	Unit	Timing diagram	Min	Typ	Max
Reset "Low" level width	tRES	us	Figure 11.2.-3	10	-	-
Reset rise time	trRES	ns	Figure 11.2.-3	-	-	10

※ When Reset L-period is less than about 5usec, reset function don't work.